COMPREHENSIVE COMPACT NOISE MODELING
OF NANOSCALE CMOS DEVICES

By

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A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

UNIVERSITY OF FLORIDA

2003

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ACKNOWLEDGMENTS

I would like to acknowledge my advisor, Professor Gijs Bosman, for his encouragement and support throughout the course of this work. He has been a great research mentor with his unswerving guidance, enthusiasm, and management skills. He also has been instrumental to my education and research, playing an exceptional role model of life. It has been memorable that he did his utmost to help with concern and encouragement. I also would like to thank the members of my supervisory committee, Professors Sheng S. Li, William R. Eisenstadt, and Cammy R. Abernathy, for their guidance and interest in this work. I thank Marcy Bryant, Erlinda Lane, and Edna Hamilton for all of their help preparing presentations and arranging travel plans for conferences and reviews, and Linda Kahila for administrative guidance.

I would also like to thank the Semiconductor Research Corporation (SRC) and the University of Florida for their financial support, as well as Texas Instruments (TI) Inc. for providing MOS devices and noise data. I am also grateful to industrial liaison, Keith R. Green of TI and Rainer Thomas of Motorola for their research guidance and interest. I also want to thank D. Ladwig of TI for noise measurement and C-V data. Special thanks go to my colleagues in the Noise Research Laboratory, D. Martin, F. Hou, J. Sanchez, and L. Kore, for their encouragement and useful technical discussions.

I would also like to thank Jaeseok Kim for his help in implementing the noise model into BSIM4, and fellow students Byungseo Kim, Sanghoon Choi, Sungphil Kim,

Dongho Han, Yooseok Ko, Hyungjong Ko, Namkyu Park, Dongjoon Yang, Sungmo Yim, Byumjin Park, Hanjo Kim, Seeyoo Nho, Jihoon Yang, Kyukil Choi, Joonhee Moon, and Jiyun Song for their daily companionship and informative discussions. I also wish to thank Al Ogden and Steven Schein for their assistance in making devices for noise measurements. Also, thanks go to all of the friends that have made my four years at the University of Florida such as an enjoyable chapter of my life.

Specially, I am deeply indebted to my family members-my father, my mother, my brothers, my sisters, my parents-in-law, my brothers-in-law, my sisters-in-law, my nieces, my nephews, and my wife. I am deeply thankful to my parents who gave me unconditional and unceasing support and stressed the importance of education to me, and my parents-in-law for their genial favor and emotional support. In particular, I am grateful to my eldest brother, Jongchan Lee, for his constant encouragement and support in my academic pursuits. My sincere appreciation must be reserved for my lovely wife, Eunsil Choi, for her sacrifice and unwavering love to me. Finally, this work is dedicated to my God.

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Abstract of Dissertation Presented to the Graduate School
of the University of Florida in Partial Fulfillment of the
Requirements for the Degree of Doctor of Philosophy

COMPREHENSIVE COMPACT NOISE MODELING OF NANOSCALE CMOS DEVICES

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May 2003

Chair: Dr. Gijs Bosman
Major Department: Electrical and Computer Engineering

The dissertation focuses on the physics-based compact noise modeling of nanoscale complementary metal-oxide-semiconductor (CMOS) devices. The models are primarily developed to be implemented in circuit simulators, and are further applied to gain insight into the noise behavior of advanced metal-oxide-semiconductor field-effect transistors (MOSFETs). For a comprehensive evaluation of noise performance, the models describe all the important physical noise sources and effects which are observed in nanoscale MOSFETs with ultrathin gate oxides. The models account for the gate leakage current and noise, the drain current and noise, the cross correlation effects between the gate and the drain, and quantum mechanical (QM) effects in the inversion layer.

The gate leakage current model for ultrathin nitrided oxide MOSFETs is presented, and is based on inelastic trap-assisted tunneling (ITAT) combined with a semi-empirical direct tunneling current model. In order to explain the excess noise behavior due to the gate leakage current, the low and high frequency noise models are formulated by using a barrier height fluctuation model and Lorentzian-modulated shot noise model, respectively. Trap-related processes are the most likely cause of excess current noise because slow traps in the oxide result in low frequency dissipation in the conductance of oxides, and fast traps produce the Lorentzian-modulated shot noise associated with generation-recombination (G-R) process at higher frequencies. In addition, the $1/f^{\gamma}$ noise of the gate leakage current can be used to extract the trap properties and its source is identified by the low frequency plateau in measured conductance loss. By using the partition noise theory and the BSIM4 partition current model, the cross correlation effects between the gate and the drain are modeled at low frequencies, enabling the overall noise performance to be evaluated. Furthermore, by incorporating the effects of a realistic trap distribution, the parasitic resistance, the doping profile, and the quadratic mobility degradation factor on the noise behavior, a $1/f^{\gamma}$ drain current noise model for ultrathin oxide MOSFETs is formulated on the basis of the tunneling assisted-thermally activated trapping process of carriers. For more accurate and physical prediction of noise behavior in ultrathin (≈1.5nm) MOS devices, the QM effects on the noise characteristics are taken into account. Especially, the compact noise model of gate leakage current is newly implemented into BSIM4, and the modeling is validated through a comparison of simulation results and measurements.

CHAPTER 1
INTRODUCTION

1.1 Motivation

With the steady advances in semiconductor technologies, the capability of the integrated circuit (IC) has accelerated in accordance with Moore's law [Fra01, Iwa99, Tau97]. According to the 2001 International Technology Roadmap for Semiconductors (ITRS-2001), it is projected for complementary metal-oxide-semiconductor (CMOS) technology that 64-Gb dynamic random access memory (DRAM) with gate lengths down to 10 nm is produced around 2016 [Sia01]. The continued scaling of CMOS technology has driven progress in very large scale integration (VLSI) applications. However, as the downsizing of the components of VLSI circuits, such as the MOS field-effect transistor (MOSFET), continues, it is expected to encounter physical and technological problems pertaining to scaling of CMOS devices into the nanometer regime. One of the key issues is leakage current and its associated noise [Sia01].

For very small MOSFETs, the tunneling currents present the limits to useful device operation [Fra01]. The most constraining limit to scaling is the tunneling current through the gate insulator. The resulting gate leakage currents make the use of ultrathin oxides (<2nm) impractical in many device applications where high performance and low standby power consumption are required. Moreover, the thin gate oxide is associated with the loss of inversion charge, and thus transconductance, due to inversion layer quantization and polysilicon-gate depletion effects [Tau97]. Another possible source of

Table 1.1 Low operating power (LOP) logic technology requirements (ITRS – 2001 Edition)

Year of Production	Physical Gate Length (nm)	Physical EOT*, $t_{ox,physical}$ (nm)	Electrical EOT*, $t_{ox,electrical}$ (nm)	Subthreshold Leakage Current, $I_{sd,leak}$(pA/μm)	Power Dissipation per Device** (W/Device)
2001	90	2.0 – 2.4	3.0	100	3.2×10^{-11}
2002	75	1.8 – 2.2	2.8	100	2.9×10^{-11}
2003	65	1.6 – 2.0	2.6	100	2.1×10^{-11}
2004	53	1.4 – 1.8	2.4	300	5.2×10^{-11}
2005	45	1.2 – 1.6	2.2	300	4.1×10^{-11}
2006	37	1.1 – 1.5	2.1	300	3.3×10^{-11}
2007	32	1.0 – 1.4	1.7	700	6.0×10^{-11}
2010	22	0.8 – 1.2	1.5	1000	5.3×10^{-11}
2013	16	0.7 – 1.1	1.4	3000	1.0×10^{-10}
2016	11	0.6 – 1.0	1.3	10000	2.0×10^{-10}

* $t_{ox,electrical} = t_{ox,physical} + (\varepsilon_{ox} / \varepsilon_{si}) x_n^{QM}$, where x_n^{QM} is the actual charge position from the interface.

** Static power dissipation for an nMOS device with dimension $W/L_{gate} = 3$.

leakage current is the direct subthreshold source-to-drain tunneling through the potential barrier below the gate [Fra01], as shown in Table 1.1. For low power MOS transistors, the subthreshold source-to-drain leakage current $I_{sd,leak}$ increases quite rapidly with succeeding years, owing to the reduction of the threshold voltage. This increase in $I_{sd,leak}$ causes the static power dissipation per device to increase somewhat with device scaling, despite the reduction in the power supply voltage and the device dimension with scaling. Since the gate leakage current must remain less than $I_{sd,leak}$, a reasonable restriction is imposed on it. Because of the large increases in $I_{sd,leak}$ with device scaling, it is expected that heavily nitrided oxy-nitrides are sufficient to meet the gate leakage requirements until the end of the roadmap. Given the required equivalent oxide thickness (EOT) in 2005, however, the gate leakage current targets cannot be met using oxy-nitride because of direct tunneling through the gate oxide. Furthermore, there are serious issues of thickness control and uniformity for ultrathin oxy-nitride gate dielectrics, and reliability issues, especially with large gate leakage current. From the standpoint of static power dissipation control, it is also desirable to reduce the gate leakage current.

Although remarkable improvements in CMOS technologies have been made in the past 20 years, noise is always one of the most constraining limits to scaling. Due to its origin in the basic mechanisms which are responsible for the conduction of current through devices, noise is inevitable even in scaled MOSFETs. Generally, the continuous minimization of MOS deices causes a significant increase in noise amplitude, leading the feasibility of nanoscale MOS devices to be questioned [Bou98, Cel99, God97]. If the noise sources are uniformly distributed over the gate area, the noise spectral density is inversely proportional to the area [Sim99]. Also, the device-to-device fluctuations in the $1/f$ noise performance increase in the small geometry devices. For ultrathin oxide MOS devices, it is obvious that the gate leakage tunneling current is the origin of low frequency noise sources, and adversely affect the noise characteristics [Lee02, Mom98]. In order to reduce the gate leakage current, the present gate oxide dielectric will eventually be replaced by alternative materials with different trap properties and potential barriers. In that case, the low frequency noise becomes a more significant issue, since the noise is strongly affected by the physical properties of the gate insulator, such as trap density, trap distribution, and tunneling effects. In addition, the low frequency noise in ultrathin MOS devices can be also used as a sensitive probe for investigating localized

Table 1.2 Mixed-signal device technology requirements (ITRS – 2001 Edition)

Year of Production	Physical Gate Length (nm)	NMOS RF Device		NMOS Analog Device	
		T_{ox} (nm)	*1/f* noise* ($\mu V^2 \mu m^2/Hz$)	T_{ox} (nm)	*1/f* noise* ($\mu V^2 \mu m^2/Hz$)
2001	65	1.3 - 1.6	500	2.5 – 7.0	1000
2002	53	1.2 - 1.5	500	2.5 – 7.0	500
2003	45	1.1 – 1.6	300	2.5 – 5.0	500
2004	37	0.9 – 1.4	300	2.5 – 5.0	500
2005	32	0.8 – 1.3	300	2.5 – 5.0	300
2006	28	0.7 – 1.2	200	2.5 – 5.0	300
2007	25	0.6 – 1.1	200	2.5 – 5.0	300
2010	18	0.5 – 0.8	150	1.3 – 3.0	150
2013	13	0.4 – 0.6	100	1.3 – 3.0	100
2016	9	0.4 – 0.5	75	1.3 – 2.5	100

* *1/f* noise spectral density, at a frequency of 1Hz, normalized to an active area of 1 μm^2. Operation point taken at 100 mV above the threshold voltage

phenomena, such as degradation and failure in IC, because the noise and/or fluctuations are influenced by the presence of localized defects and irregularities in the microstructure of devices [Cio00]. Furthermore, in the field of mixed-signal integrated circuits containing analog and/or radio frequency (RF) circuitry as well as the digital circuitry, continuous focus on *1/f* noise is imperative to satisfy the increasing demands on noise limitation. The *1/f* noise of digital MOS devices at a frequency of 1Hz is critical for the minimum input signal in mixed-signal circuits (lower boundary for dynamic range) in low frequency circuits, mixers, and voltage controlled oscillators (VCOs) [Sia01]. Table 1.2 shows the mixed-signal device technology requirements (ITRS-2001 Edition). Although *1/f* noise in MOS devices due to carrier trapping-detrapping in traps at the Si-

SiO_2 interface is more prominent than in bipolar or junction field-effect transistors (JFETs), the noise requirements continue to be conflicting with succeeding years.

Noise modeling is important for understanding the noise behavior and optimizing the low noise designs. The needs for noise modeling are driven by the continuous reduction of feature size in scaling MOSFETs, which not only causes higher demands on model accuracy but also requires models for currently not considered material properties. Two models widely used in circuit simulators for MOSFETs noise are SPICE (Simulation Program for Integrated Circuits Emphasis) and BSIM (Berkeley Short-channel IGFET Model) noise models. The SPICE model is largely empirical and is considered to be oversimplified. The lack of a systematic approach for determining the empirical parameters imposes another serious limitation in using the model. The BSIM *1/f* noise model for drain current is a physics-based model applicable to all MOSFET operation regimes, which incorporates both carrier number fluctuation and surface mobility fluctuation [Hun90a, Hun90b]. However, this model is at best 10 years old. In addition, the direct tunneling gate current model of BSIM not only underestimates the current magnitude in ultrathin nitrided oxide devices, but also there is no noise model for the gate leakage current. Due to the impact of gate leakage current on the overall noise performance, a comprehensive noise model is required covering each important noise source over the entire frequency range. Furthermore, since the small size and high doping concentration create quantized energy levels within the channel, noise models accounting for quantum-mechanical (QM) effects are indispensable in nanoscale MOSFETs. It should also be noted that a key difficult challenge across all the noise modeling area is that of experimental validation. As devices shrink and become vulnerable, new noise measurement techniques that provide the necessary information for the validation of models are critical. It is clear from the above that in order to consider advanced CMOS device and technology changes made during the last decade, the present noise models should be replaced by more accurate physics-based noise models which account for 1) gate leakage current effects, 2) correlation effects between the gate and the drain, 3) short channel effects, 4) realistic trap properties, 5) QM effects observable in carrier-trap interaction, and 6) experimental validation.

1.2 Overview of Noise Sources

The design of low noise MOSFET devices and/or circuits can be achieved, if the fundamental noise models of devices are developed and understood in the light of physical origin of noise sources. Four important kinds of noise sources in MOSFETs are thermal noise, shot noise, generation-recombination (GR) noise, and 1/*f* noise, as illustrated in Figure 1.1.

1) Thermal noise, Nyquist noise, or Johnson noise of MOSFETs is due to the random thermal motion of the charge carriers in the channel. It produces a fluctuating current at the device terminals. Under thermal equilibrium, the thermal noise can be obtained either from drift or diffusion carrier transport mechanisms. The MOSFET thermal noise expression for the drain current I_d that is widely used in the literature and in circuit simulators is

$$S_{I_d}^{T}(f) = \gamma_T \cdot 4kTg_{d0} \tag{1.1}$$

where k is Boltzmann's constant, T is the absolute temperature, g_{d0} is the channel conductance with zero drain-to-source voltage, with $2/3 < \gamma_T < 1$ in the linear region, and

$\gamma_T = 2/3$ in the saturation region for long channel device. Thermal noise is called a white noise at low frequencies, because its power spectral density is flat up to extremely high frequencies of over 10^{12} Hz. In addition to channel thermal noise in MOS devices, two additional thermal noise sources are the gate poly resistance and the bulk resistance.

2)) Shot noise is generated when charge carriers encounter a potential barrier and cross barriers independently and at random. The power spectral density for the gate leakage current I_g in ultrathin oxide MOSFETs is given by

$$S_{I_g}^{S}(f) = F^{Fano} \cdot 2qI_g \tag{1.2}$$

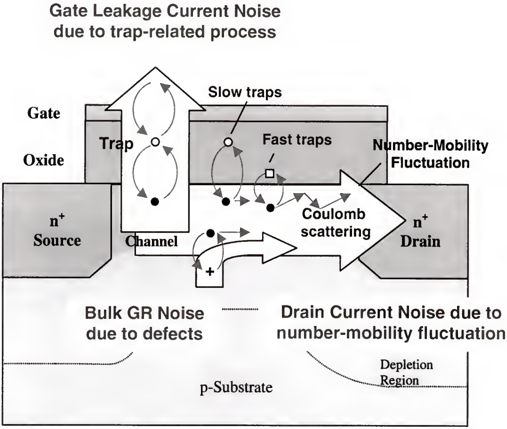


Figure 1.1 Charge transport and physical origin of noise sources in MOSFET

The power spectral density is constant up to $f \approx 1/\tau_{trans}$ with τ_{trans} the transit time across the barrier. The analysis of shot noise is performed by introducing the Fano factor F^{Fano} defined as $F^{Fano}=S_{Ig}/(2qI_g)$ where I_g is the current leakage flowing in the gate. Shot noise suppression ($0<F<1$) is associated with a negative correlation between current pulses due to Coulomb interaction and the Pauli exclusion principle [Ian97, Ian98, Ian00]. In contrast, shot noise enhancement is associated with a positive correlation between current pulses.

3) Generation-recombination (GR) noise is due to fluctuations in the number N of electrons and holes in the conduction and valence bands, respectively. These fluctuations in the number of free carriers are caused by the trapping-detrapping of carriers to either bulk or surface defect centers. Each trap center is characterized by its energy level, trap density, and carrier capture coefficients. The power spectral density of the fluctuations in N is given by

$$S_N^{GR}(f) = 4\,\overline{\Delta N^2}\,\frac{\tau}{1+4\pi^2 f^2 \tau^2} \tag{1.3}$$

where τ is the relaxation time constant of the trapping process, $\overline{\Delta N^2}$ is the variance of the fluctuations ΔN, and f is the frequency. The spectrum appears to be constant at low frequency, then drops off as $1/f^2$ above the corner frequency, which is determined by the trap characteristic time. If the GR noise stems from one single trap, it is called random telegraph signal (RTS) noise. As shown in Figure 1.1, GR noise in MOSFETs is due to random trapping-detrapping of carriers at the defect or impurity centers in the depletion region between the conductive channel and the semiconductor substrate. The GR noise component is usually overshadowed by the higher $1/f$ surface noise component. However, there have been several reported instances where special device processing has led to the GR noise component dominating [Fan86].

4) *1/f* noise or flicker noise owes its name to its spectral density that is almost inversely proportional to the frequency over a wide frequency range down to very low frequencies as follows :

$$S_I^{1/f}(f) = KF \cdot \frac{I^{AF}}{f^{\gamma}} \tag{1.4}$$

where γ is the frequency exponent, whose value usually lies in the interval between 0.7 and 1.3, and *KF* and *AF* are the magnitude coefficient and the current exponent, respectively. As depicted in Figure 1.1, the physical origins of *1/f* noise of drain current in MOSFETs can be explained by two major models. The number fluctuation model, originally proposed by McWhorter, attributes *1/f* noise to the random trapping and detrapping processes of charge carriers in the oxide traps near the Si-SiO$_2$ interface [McW57]. It is assumed that only traps within a few *kT* of the Fermi-level are effective in generating noise and the channel can exchange charges with the oxide traps through tunneling, as shown in Figure 1.2. The trapping and detrapping in these traps produce GR spectra with distributed relaxation times. Since the *1/f* or $1/f^{\gamma}$ noise spectrum is the result of a weighted superposition of RTS events, the studies of RTS's have greatly contributed to our understanding of the nature of *1/f* noise in MOSFETs. The mobility fluctuation model, based on Hooge's relationship, considers *1/f* noise as a result of the fluctuation in bulk mobility due to carrier scattering at lattice vibrations. Since in this process no traps are needed, this model implies that there is *1/f* noise even if no traps are present. In addition, a unified model has been developed in order to explain a broader set of data

[Ghi91, Hun90a, Hun90b, Jay89]. This model is based on the fact that fluctuation in the occupancy of the oxide traps induces correlated fluctuations in the carrier number and surface mobility [Hun90c].

From the standpoint of noise sources in ultrathin oxide MOSFETs, the equivalent input noise current power $S_{I,eq}(f)$ and voltage power $S_{V,eq}(f)$ are given by, respectively

$$S_{I,eq}(f) = S_{I_g}^{S}(f) + S_{I_g}^{1/f}(f) + \frac{(2\pi f C_{gs})^2}{g_m^2}\left[S_{I_d}^{T}(f) + S_{I_d}^{1/f}(f)\right] \tag{1.5a}$$

$$S_{V,eq} = \frac{1}{g_m^2}\left[S_{I_d}^{T}(f) + S_{I_d}^{1/f}(f)\right] \tag{1.5b}$$

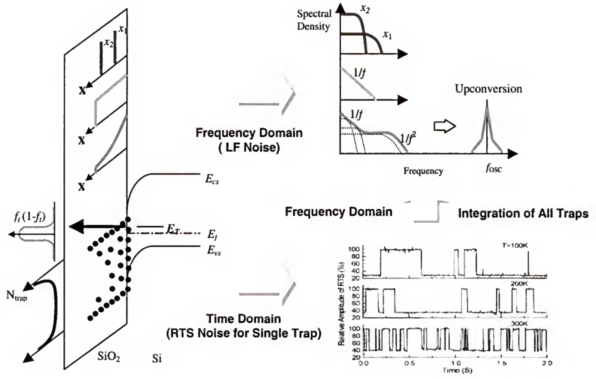


Figure 1.2 Noise spectrum and trap distributions in MOS structure

where C_{gs} is the gate-to-source capacitance and g_m is the transconductance. The equivalent input noise current at low frequencies is dominated by the *1/f* noise $S_{I_g}^{1/f}(f)$ and shot noise $S_{I_g}^{S}(f)$ due to the gate leakage current, as shown in Figure 1.3. Thus, the total input noise voltage can be expressed as

$$S_{V,in}(f) = S_{V,eq}(f) + S_{I,eq}(f)|Z_s|^2 + 2\sqrt{S_{V,eq}(f) \cdot S_{I,eq}(f)}\,\mathrm{Re}\left[C(f) \cdot Z_s^*\right] \qquad (1.6)$$

where Z_s is the complex impedance and $C(f)$ is the correlation coefficient. Due to the presence of the gate leakage current, the total input noise voltage contains the correlated noise component caused by the common noise sources. These effects have to be taken into account for accurate prediction of the noise performance in ultrathin oxide MOSFETs.

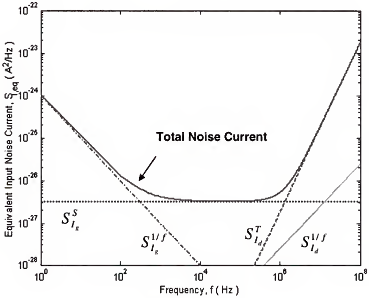


Figure 1.3 Equivalent input noise current components in ultrathin oxide MOSFETs showing different frequency dependencies.

1.3 Organization

In this dissertation, a detailed study of the physics-based compact noise models in nanoscale MOSFETs will be presented, as outlined in Figure 1.4. In Chapter 2, an analytical model of the gate leakage current in ultrathin gate nitrided oxide MOSFETs is presented. This model is based on an inelastic trap-assisted tunneling (ITAT) mechanism combined with a semi-empirical gate leakage current formulation. The tunneling-in and tunneling-out currents are calculated by modifying the expression of the direct tunneling current model of BSIM (Berkeley Short-channel IGFET Model). For a microscopic interpretation of the ITAT process, resonant tunneling (RT) through the oxide barrier containing potential wells associated with the localized states is proposed. We employ a quantum-mechanical model to treat electronic transitions within the trap potential well. The ITAT current model is then quantitatively consistent with the summation of the resonant tunneling current components of resonant energy levels. Moreover, the proposed ITAT process is supported by the low frequency excess noise components. The $1/f$ noise observed in the gate leakage current implies the existence of slow processes with long relaxation times in the oxide barrier. In order to verify the proposed ITAT current model, an accurate method for determining the device parameters is necessary. The oxide thickness and the interface trap density of the gate oxide in the 20-30 Å thickness range are evaluated by the quasi-static C-V method, dealing especially with quantum-mechanical and polysilicon effects.

Chapter 3 presents a physics-based analytical model of the gate leakage current noise in ultrathin gate oxide MOSFETs. On the basis of the gate leakage current mechanisms, we employ a barrier height fluctuation model and the Lorentzian modulated shot noise of the gate leakage current stemming from the two dimensional electron gas channel to explain the excess noise behavior. The excess noise can be interpreted as the sum of $1/f^\gamma$ noise and the Lorentzian modulated shot noise. Trap-related processes are the most likely cause of excess current noise because slow traps in oxide can result in low frequency dissipation in the conductance of oxides, and fast traps produce the Lorentzian-modulated shot noise associated with generation-recombination (G-R) process at higher frequencies. In order to verify the proposed noise model, the simulation results are compared with experimental data, and excellent agreement is observed. The noise model can accurately predict the excess noise behavior of MOSFETs with ultrathin gate oxide and is particularly suitable to be implemented in circuit simulators.

In Chapter 4, the electrical trap properties in ultrathin oxide MOSFETs are extracted using $1/f^\gamma$ low frequency noise components of gate leakage current. The technique is based on low frequency noise measurements which are capable of probing trap states over energy and space. The gate voltage is swept between 0.4 and 1.32 V to obtain the different power slopes γ of the $1/f^\gamma$ noise spectrum. From the measured noise data, trap parameters such as the slow trap densities and capture cross section are accurately determined as a function of trap energy and trap distance. The $1/f^\gamma$ noise measurement results confirm that the capture cross sections depend strongly on the surface potential, and the slow trap densities estimated near the band edge and at the Si-SiO_2 interface are higher than those near the midgap and at deeper distance. Moreover, the parallel conductance spectroscopy of slow traps is reproduced by $1/f^\gamma$ low frequency noise measurements, and is verified by the low frequency plateau in measured conductance loss $G_p(f)/w$. For the purpose of investigating the dependency of trap parameters on the complex admittance of oxide traps, the Cole-Cole plots for different trap profiles, a uniform and exponentially decreasing trap distribution in space, are calculated using the theoretical model. The noise spectroscopy technique further reveals the dynamic evolution of trap states and gives a clear physical understanding of the pertinent low frequency noise sources.

In Chapter 5, an analytical model and analysis of the low frequency noise performance of ultrathin oxide MOSFETs are presented. The model includes the effects of gate tunneling leakage current, low frequency noise sources, and their cross correlation coefficient between the input and the output. The correlation coefficient is not negligible in the existence of direct tunneling current through the gate oxide, and has an impact on the overall noise performance at low frequencies. Based on the partition noise theory and the BSIM4 gate leakage current model with the source-drain partition, the correlation coefficient is obtained from a physical and rigorous modeling of intrinsic noise sources. The calculated results are compared with correlation noise measurements and good agreement is observed. An analytical formulation of low frequency noise performance is newly derived using the frequency-dependent noise parameters P^{LF}, R^{LF}, and C^{LF}. Noise performance parameters, such as minimum noise figure, optimum source resistance and reactance, are graphically presented to accurately predict the influences of the gate leakage current on the low frequency noise performance. From quantitative results simulated with typical device parameters, it is shown that the proposed model can be used for optimum designs of ultrathin oxide MOS devices and circuits at low frequencies.

Chapter 6 presents a $1/f^{\gamma}$ drain current noise model for deep-submicron MOSFETs with ultrathin oxide. Based on the number and correlated mobility fluctuation mechanisms, the model is derived incorporating a tunneling assisted-thermally activated process and a realistic trap distribution inside the gate oxide layer. The effects of the device structure and processing technologies on the noise characteristics are taken into consideration through a quadratic mobility degradation factor, a parasitic resistance, a doping profile, and trap-related parameters. For ultrathin oxide MOSFETs, the trapping efficiency ratio and the scattering rate are expressed in terms of the trap distance and the inversion carrier density, enabling an accurate prediction of the noise behavior. The model parameters are extracted and determined so that the model has an excellent agreement with the measured data for advanced MOSFETs operating in both the linear and saturation regions. From quantitative results simulated with the extracted data, it is shown that the new model is applicable to the design of future CMOS devices and new device processing technologies, and is suitable to be implemented in circuit simulators.

In Chapter 7, a charge-based quantum correction model for current and noise in nanoscale MOSFETs is presented. The model is analytically formulated by incorporating quantum mechanical (QM) effects in the inversion layer into the current and noise models of BSIM. For efficient computation, the quantum correction models are calculated for the lowest quantized energy level, which is a reasonable approximation. The QM effects on the inversion charge parameters, such as the surface potential, the threshold voltage, the inversion charge density, and the gate capacitance model, are taken into account. On the basis of the quantum correction model of the oxide voltage and oxide thickness, the gate leakage tunneling current and $1/f$ noise model are evaluated for ultrathin gate oxide MOS devices. The quantum models of the drain current and noise are obtained by accounting for the QM effects through the inversion charge density model.

Quantitatively, it is confirmed that the quantum correction of the oxide thickness is essential to the accurate prediction of the gate leakage current and noise model. For the $1/f$ drain current noise due to the number fluctuation components, the classical and QM models behave in a qualitatively similar fashion to the RTS noise in both the weak and strong inversion, showing a noticeable deviation in the saturation region. It is also shown that QM effects in the inversion layer are important to the thermal noise modeling and, for the accurate noise modeling of nanoscale MOSFETs, become more pronounced for higher doping concentration and thinner oxide thickness.

In Chapter 8, the comprehensive and physics-based compact noise models for advanced CMOS devices are presented. The models incorporate all the important physical effects of nanoscale MOSFETs, and are formulated to be suitable for circuit simulators. Especially, the implementation of the gate leakage current and noise models in BSIM4 is demonstrated.

Finally, Chapter 9 summarizes the primary contributions of this work and then concludes with suggestions to further advance noise models to design future CMOS devices.

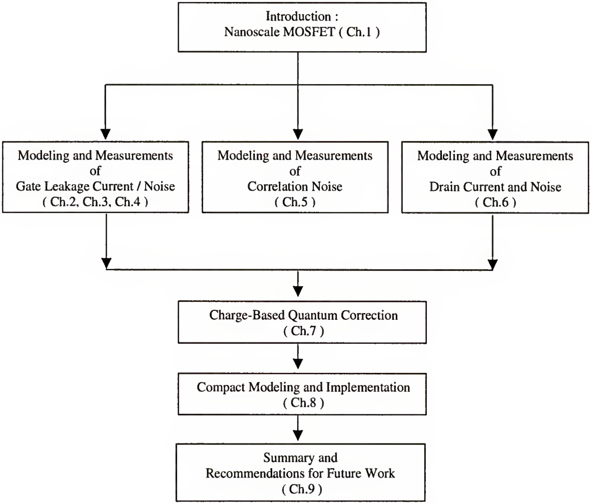

Introduction :
Nanoscale MOSFET (Ch.1)
Modeling and Measurements of Gate Leakage Current / Noise (Ch.2, Ch.3, Ch.4)
Modeling and Measurements of Correlation Noise (Ch.5)
Modeling and Measurements of Drain Current and Noise (Ch.6)
Charge-Based Quantum Correction (Ch.7)
Compact Modeling and Implementation (Ch.8)
Summary and Recommendations for Future Work (Ch.9)

Figure 1.4 Organization and overview of this dissertation

CHAPTER 2
GATE LEAKAGE CURRENT MODEL AND ANALYSIS

2.1 Introduction

Advancement of VLSI technologies has resulted in continuous scaling down of MOS devices, whose feature size used in IC chips has been reduced to deep-submicron nowadays. At the same time, the continuous reduction of the gate oxide layer thickness in advanced CMOS devices leads to excessive gate leakage currents and reliability problems [Ner95, Sch94a, Sch94b]. For such ultrathin oxide layers, the gate tunneling current is one of the limiting factors for future MOS technologies because a significant tunneling current is expected even at normal operating conditions. This large tunneling current increases stand-by power consumption and deteriorates device performance [Ghe00a, Ghe00b]. Moreover, the gate leakage current in ultrathin gate oxide MOS devices should be considered as a low frequency noise source [Mom98].

Nitridation treatment of thin oxides is used in MOS technology to improve the dielectric robustness to electrical stress and to develop high permittivity gate dielectric stacks. However, one of the problems associated with the nitridation process is that it introduces a large number of electron traps into the insulating layer [Che88]. It was shown that the enhanced current in nitrided oxide and high dielectric stacks are mainly due to two-step trap-assisted tunneling [Che88, Fle92, Fle93, Hou99, Yan96]. Since energy loss has been observed during tunneling through gate oxides, an inelastic process has to be incorporated in these trap-assisted tunneling models [Tak99]. Endoh *et al.*

proposed an analytical ITAT model for stress-induced leakage current (SILC) in 6.8 nm thick silicon dioxide films, describing the quantitative analysis of trap-related properties [End99]. However, a conclusive ITAT current model in the direct tunneling regime at low voltages has not been established [Ghe00b].

In order to provide a better physical understanding of ITAT mechanisms, a microscopic interpretation is necessary. Both Coulombic and neutral trapping sites in SiO_2 used in MOS technologies have been found to be responsible for leakage current and noise mechanisms [Buc91, Mom98]. Cheung et al. showed that tunneling is enhanced by a localized point defect and resonant tunneling may be the missing physical picture [Che97]. If we treat the trapping states as the discrete levels of the quantum wells associated with the defects [Buc91], a theory of resonant tunneling through localized trapping sites can be applied to the ITAT current modeling [Bro92, Buc88, Ric84]. In addition, it has been shown that the inelastic scattering process involved in the ITAT is producing low frequency noise [Ma92].

Accurate and efficient methods for determining the gate oxide thickness and trap density are indispensable for device modeling and process monitoring. The gate oxide thickness is reaching a range where quantum-mechanical (QM) effects should not be neglected [Cle00, Dmo97, Omu00]. QM effects mainly affect the energetic and spatial carrier distribution in inversion layers, which induce significant modifications in the CV characteristics and modeling. Moreover, the polysilicon gate effect, which results in the creation of a space charge in the gate region, results in anomalous CV characteristics [Qud00]. All these effects have to be taken into account and evaluated for the accurate extraction of device parameters.

In this Chapter, we will present a detailed study of a physics-based compact model for the gate leakage current in ultrathin gate nitrided oxide MOSFETs. In Section 2.2, an ITAT model is proposed to characterize the observed conduction enhancement. This model is based on inelastic trap-assisted tunneling combined with a semi-empirical direct tunneling current step. In Section 2.3, resonant tunneling through the oxide barrier containing potential wells associated with the electronic defect states is proposed as a microscopic interpretation of the ITAT process. Section 2.4 shows how the characterization and modeling procedure can be applied to devices featuring ultrathin nitrided oxides for the purpose of validating the leakage tunneling current model from C-V, I-V, and noise measurements. Finally, Section 2.5 presents some conclusions.

2.2 Modeling of Gate Leakage Current

2.2.1 Direct Tunneling Gate Leakage Current

When the oxide layer is thicker than 6 *nm* and the applied field is in the Fowler-Nordheim (FN) region, the leakage current can be explained by FN electron tunneling in MOS structures [Dep95]. For an ultrathin oxide layer and an applied voltage below the potential barrier height, the classical FN formula is not applicable. From an independent electron approximation and for an elastic tunneling process, the direct tunneling current density from the Si inversion layer to the poly-Si gate can be expressed as [Dep95]

$$J_{DT}(\phi_b, F_{ox}) = \frac{A}{\alpha(\phi_b, F_{ox})} F_{ox}^2 \exp\left[-\frac{B}{F_{ox}}\beta(\phi_b, F_{ox})\right] \tag{2.1}$$

with

$$\alpha(\phi_b, F_{ox}) = \left[1-\sqrt{\frac{\phi_b - qV_{ox}}{\phi_b}}\right]^2 = \left[1-\sqrt{1-\gamma F_{ox}}\right]^2 \tag{2.2a}$$

$$\beta(\phi_b, F_{ox}) = \frac{\phi_b^{3/2} - (\phi_b - qV_{ox})^{3/2}}{\phi_b^{3/2}} = 1-(1-\gamma F_{ox})^{3/2} \tag{2.2b}$$

$$\gamma = \frac{qt_{ox}}{\phi_b}, \qquad F_{ox} = \frac{V_{ox}}{t_{ox}}, \qquad A = \frac{q^3}{16\pi^2 \hbar \phi_b}, \qquad B = \frac{4}{3}\frac{\sqrt{2m_{ox}}}{q\hbar}\phi_b^{3/2} \tag{2.2c}$$

where q is the electron charge, ϕ_b is the energy barrier height, $\hbar$ is the reduced Planck constant, t_{ox} is the oxide thickness, m_{ox} is the electron effective mass of the conduction band in the oxide, and F_{ox} is the electric field in the oxide layer. In order to calculate the gate tunneling currents through thin oxides, it is necessary to relate the oxide voltage V_{ox} to the applied gate voltage V_g, since V_{ox} depends on V_g as well as the surface potential ψ_s and the polysilicon voltage drop as follows

$$V_{ox} = V_g - V_{FB} - \psi_s - V_{poly} \tag{2.3}$$

An accurate computation of V_{ox} for a given V_g requires accounting for the voltage drop across the polysilicon gate due to the formation of a depletion layer near the poly-SiO$_2$ interface. For a positive voltage applied to an n$^+$ polysilicon gate with the p-substrate grounded, the polysilicon will deplete. The value of V_{poly} is given by [Qud00]

$$V_{poly} = \frac{1}{2m}\left[2mV_g^{'} + 1 - \sqrt{1 + 4mV_g^{'}}\right] \tag{2.4}$$

with

$$m = \frac{\varepsilon_{ox}^2}{2\varepsilon_{Si} q N_{poly} t_{ox}^2}, \qquad V_g^{'} = V_g - V_{FB} - \psi_s \tag{2.5}$$

where N_{poly} is the polysilicon doping concentration and V_{FB} is the flat-band voltage.

The BSIM4 model can predict all the significant direct tunneling current components which are electron tunneling from the conduction band in the substrate to the gate, electron tunneling from the valence band in the substrate to the gate, and hole tunneling from the valence band in the gate to the substrate. The BSIM4 gate oxide tunneling current model is given by [Lee00, Yeo00]

$$J_{DT,BSIM} = \frac{q^3}{8\pi h \phi_b \varepsilon_{ox}} \cdot C(\phi_b, t_{ox,} F_{ox}, V_g) \cdot \exp\left[-\frac{8\pi\sqrt{2m_{ox}}\,\phi_b^{3/2}[1-(1-|V_{ox}|/\phi_b)^{3/2}]}{3hq|F_{ox}|}\right] \quad (2.6)$$

This formula is very similar to Equation (2.1) except for the correction function C ($V_g, V_{ox}, t_{ox}, \phi_b$) as expressed by [Lee00, Yeo00]

$$C(\phi_b, t_{ox}, F_{ox}, V_g) = \exp\left[\frac{20}{\phi_b}\left(\frac{t_{ox}|F_{ox}|-\phi_b}{\phi_{bo}}+1\right)^{\lambda} \cdot \left(1-\frac{t_{ox}|F_{ox}|}{\phi_b}\right)\right] \cdot \left(\frac{V_g}{t_{ox}}\right) \cdot N \quad (2.7)$$

where λ is a fitting parameter for three current components, ϕ_{bo} is the Si-SiO$_2$ barrier height (3.1 eV for electrons and 4.5 eV for holes), ϕ_b is the tunneling barrier height, and the function N is an indicator of the density of either tunneling carrier.

2.2.2 Inelastic Trap-Assisted Tunneling (ITAT) Model

We formulate an improved model to account for the gate leakage current of MOSFETs with ultrathin gate nitrided oxides. This model combines the inelastic trap-assisted tunneling mechanism with the semi-empirical gate leakage current model of BSIM described above. The inelastic trap-assisted tunneling component describes electrons tunneling to deep-lying trap states and, immediately, released to positions deeper than the original position and subsequently tunneling to the gate under the influence of the applied electric field [Tak99]. In this process, the tunneling-in current from the inversion layer to the traps and the tunneling-out current from the traps to the gate are calculated by modifying the formulation of direct tunneling in the BSIM model. Figure 2.1 shows the schematic band diagram of two-step inelastic trap-assisted tunneling. In the capture tunneling step, the electrons undergo a direct tunneling process into the trap sites with a tunneling probability T_{DTst}. They reach the gate via an additional direct tunneling step with a probability T_{DTtg}. The tunneling probabilities T_{DTst} and T_{DTtg} are related to the tunneling-in current J_{DTin} from the inversion layer to the trap states and to the tunneling-out current J_{DTout} from the trap states to the gate. Assuming that x is the distance from the Si-SiO$_2$ interface, $N_{trap}(x,E)$ is the sheet trap density in cm^{-2} at a distance x and energy E, $f_t(x,E)$ is the electron occupancy of the traps, A_g is the gate tunneling area, and σ_t is the capture cross section of the traps, the current densities J_{DTin} and J_{DTout} are then expressed as

$$J_{DTin} = \frac{q}{A_g} g_{st}(x, F_{ox}) = \frac{q}{A_g}\sigma_t N_{trap}(x, qF_{ox1}x - \phi_b)[1 - f_t(x, qF_{ox1}x - \phi_b)]g(\phi_b, x, F_{ox1}) \tag{2.8a}$$

$$J_{DTout} = \frac{q}{A_g} r_{tg}(x, F_{ox}) = \frac{q}{A_g}\sigma_t N_{trap}(x, qF_{ox1}x - \phi_b) f_t(x, qF_{ox1}x - \phi_b)\, r(\phi_t, t_{ox} - x, F_{ox2}) \tag{2.8b}$$

$$\phi_t = \phi_b - qF_{ox1}x + E_{loss} \tag{2.8c}$$

where ϕ_t is the barrier height of the oxide trap states, and $g(\phi_b, x, F_{ox})$ and $r(\phi_b, x, F_{ox})$ are the uniform generation and recombination rate, respectively.

The resulting tunneling current J_{ITAT} of this trap-assisted tunneling process is given by a detailed balance of J_{DTin} and J_{DTout}. For an electron to contribute to the leakage current, it must first tunnel from the substrate into an intermediate trap, then tunnel out of the trap towards the gate, events which are characterized by the tunneling rates g_{st} and r_{tg}. Since both events must occur in sequence, the total tunneling rate of an

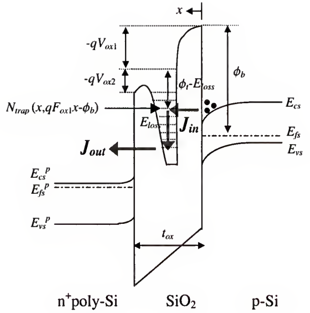


Figure 2.1 Schematic band diagram of two-step inelastic trap-assisted tunneling through the gate oxide

electron tunneling through the entire oxide via a specific trap site at a location x within the oxide can be expressed as [End99]

$$R(E,x,F_{ox})=\frac{g(\phi_b,x,F_{ox1})\cdot r(\phi_b-qF_{ox1}x+E_{loss},t_{ox}-x,F_{ox2})}{g(\phi_b,x,F_{ox1})+r(\phi_b-qF_{ox1}x+E_{loss},t_{ox}-x,F_{ox2})} \tag{2.9}$$

and

$$J_{ITAT}(E,x,F_{ox})=\frac{q}{A_g}\sigma_t N_{trap}(x,qF_{ox}x-\phi_b)\cdot R(E,x,F_{ox}) \tag{2.10}$$

The local electric fields, F_{ox1} and F_{ox2}, characterizing the separated tunneling regions can be obtained by considering the equivalent MOS capacitor circuit and using Gauss's law [End99]

$$F_{ox1} = F_{ox} + \frac{t_{ox} - x}{t_{ox}} \cdot \frac{qN_{trap}}{\varepsilon_{ox}}, \qquad F_{ox2} = F_{ox} - \frac{x}{t_{ox}} \cdot \frac{qN_{trap}}{\varepsilon_{ox}} \tag{2.11}$$

If a parabolic dispersion relation is used for the transversal energy component $E_\perp$ with a transversal electron effective mass $m_\perp$, the uniform generation and recombination rates can be represented by [Dep95]

$$g(\phi_{b1}, x, F_{ox1}) = r(\phi_{b2,} x, F_{ox2}) = \frac{4\pi m_\perp A_g}{h^3} \int_0^{E_{fs}} \int_0^{E} T_{DT}(\phi_{b1,2} - E + E_{fs}, x, F_{ox1,2}, E_\perp)\, dE_\perp dE \tag{2.12}$$

where h is the Planck constant, E_{fs} is the Fermi energy level in the Si substrate, and E is the total energy of the tunneling electron measured from the Si conduction band edge at the Si-SiO$_2$ interface. The tunneling transition probability T_{DT} for direct tunneling under the WKB approximation is given by

$$T_{DT}(E, x, F_{ox}) = \exp\left[-\frac{4\sqrt{2m_{ox}}}{3q\hbar} \cdot \frac{\left(E + \frac{m_\perp}{m_{ox}} E_\perp\right)^{3/2} - \left(E + \frac{m_\perp}{m_{ox}} E_\perp - qF_{ox}x\right)^{3/2}}{F_{ox}} \right] \tag{2.13}$$

Integrating Equation (2.12) with a substitution of a first order Taylor approximation of Equation (2.13) and introducing the correction function of BSIM, we obtain the analytical expression

$$g(\phi_b, x, F_{ox1}) = A_t \cdot \frac{C(\phi_b, x, F_{ox1})}{\phi_b} \cdot \exp\left[-B_t \cdot \frac{\phi_b^{3/2}}{F_{ox1}} \cdot \beta(\phi_b, x, F_{ox1}) \right] \tag{2.14a}$$

$$r(\phi_t, t_{ox} - x, F_{ox2}) = A_t \cdot \frac{C(\phi_t, t_{ox} - x, F_{ox2})}{\phi_t} \cdot \exp\left[-B_t \cdot \frac{\phi_t^{3/2}}{F_{ox2}} \cdot \beta(\phi_t, t_{ox} - x, F_{ox2}) \right] \tag{2.14b}$$

where

$$C(\phi_b, x, F_{ox1}) = \exp\left[\frac{20}{\phi_b}\left(\frac{x|F_{ox1}| - \phi_b}{\phi_{bo}} + 1\right)^{\lambda} \cdot \left(1 - \frac{x|F_{ox1}|}{\phi_b}\right)\right] \cdot F_{ox1} \cdot N \qquad (2.15a)$$

$$C(\phi_t, t_{ox} - x, F_{ox2}) = \exp\left[\frac{20}{\phi_t}\left(\frac{(t_{ox} - x)|F_{ox2}| - \phi_t}{\phi_{to}} + 1\right)^{\lambda} \cdot \left(1 - \frac{(t_{ox} - x)|F_{ox2}|}{\phi_t}\right)\right] \cdot F_{ox2} \cdot N$$

(2.15b)

$$\beta(\phi_b, x, F_{ox1}) = 1 - (1 - \gamma_{t1} F_{ox1})^{3/2}, \qquad \beta(\phi_t, t_{ox} - x, F_{ox2}) = 1 - (1 - \gamma_{t2} F_{ox2})^{3/2} \qquad (2.15c)$$

$$A_t = \frac{q^2 A_g}{16\pi^2 \hbar \varepsilon_{ox}}, \quad B_t = \frac{4\sqrt{2m_{ox}}}{3q\hbar}, \quad \gamma_{t1} = \frac{qx}{\phi_b}, \quad \gamma_{t2} = \frac{q(t_{ox} - x)}{\phi_t} \qquad (2.15d)$$

Putting the above equations together, the total ITAT current density J_{ITAT} is given by

$$J_{ITAT}(\phi_b, \phi_t, x, F_{ox}) = q\frac{A_t}{A_g}\sigma_t N_{trap}(x, qF_{ox}x - \phi_b) \times$$

$$\frac{\dfrac{C(\phi_b, x, F_{ox1})}{\phi_b} \cdot \exp\left[-B_t \dfrac{\phi_b^{3/2}}{F_{ox1}} \beta(\phi_b, x, F_{ox1})\right]}{1 + \dfrac{\phi_t}{\phi_b} \cdot \dfrac{C(\phi_b, x, F_{ox1})}{C(\phi_t, t_{ox} - x, F_{ox2})} \cdot \exp\left\{-B_t\left[\dfrac{\phi_b^{3/2}}{F_{ox1}} \beta(\phi_b, x, F_{ox1}) - \dfrac{\phi_t^{3/2}}{F_{ox2}} \beta(\phi_t, t_{ox} - x, F_{ox2})\right]\right\}}$$

(2.16)

This formula is a function of the local electric fields F_{ox1} and F_{ox2}, the oxide thickness t_{ox}, the barrier height of the oxide trap states ϕ_t, and the barrier height between the substrate and oxide ϕ_b. Note that this current flow through the oxide layer is valid for $V_{ox1} < \phi_b$.

2.3 Microscopic Analysis of Current Transport

Resonant tunneling (RT) through the oxide barrier containing potential wells associated with the electronic states is proposed as a microscopic interpretation of the inelastic trap-assisted-tunneling process. In order to avoid the difficulty of treating electrons classically when they are confined only a few nanometers away from the trapping sites, we can employ a quantum-mechanical model which describes the electronic states in the potential well [Buc91]. In this model, the electrons are bound to localized states, and electronic transitions from any localized state to any other occur within the trap from interactions of the electrons with phonons and photons.

If the trap state has an energy broadened level due to its interaction with the emitter states lying near the Fermi energy, then resonance tunneling can occur through a new channel where the tunneling electron goes from the emitter to the trap state, and subsequently tunnels through the reduced barrier between the trap state and collector [Ban88, Bla00, Coo86]. This resonance tunneling process causes an enhancement in the tunneling current density when the electron energy and the trap energy level line up. However, tunneling electrons suffer inelastic events in the potential well. Inelastic events lead to a broadening and decrease in the resonant transmission. The decrease of the peak transmission with increasing inelastic scattering is accompanied by an increase in the off-resonant transmission. Therefore, the theory of resonant tunneling through isolated trap states should be modified to include inelastic scattering processes occurring in the trapping state [Bla00, Bro92, But88].

In the neighborhood of a resonance, the total tunneling probability for an electron to traverse through a double barrier with a quantum well is [But88]

$$T_n^{tot}(E,x,F_{ox1},F_{ox2},p)=\sum_n T_n^{peok}(E,x,F_{ox1},F_{ox2})\frac{\Gamma_n^e(E,x,F_{ox1},F_{ox2})\Gamma_n(E,x,F_{ox1},F_{ox2},p)}{(E-E_n^{res})^2+\Gamma_n^2(E,x,F_{ox1},F_{ox2},p)} \tag{2.17}$$

with

$$T_n^{peak}(E,x,F_{ox1},F_{ox2}) = \frac{4\,T_{DTst}(E,x,F_{ox1})\cdot T_{DTtg}(E,x,F_{ox2})}{\left[T_{DTst}(E,x,F_{ox1})+T_{DTtg}(E,x,F_{ox2})\right]^2} \tag{2.18a}$$

$$\Gamma_n(E,x,F_{ox1},F_{ox2},p) = \Gamma_n^e(E,x,F_{ox1},F_{ox2}) + \Gamma_n^i(v,p) \tag{2.18b}$$

$$\Gamma_n^e(E,x,F_{ox1},F_{ox2}) = \Gamma_n^{DTst}(E,x,F_{ox1}) + \Gamma_n^{DTtg}(E,x,F_{ox2}) \tag{2.18c}$$

$$\Gamma_n^{DTst}(E,x,F_{ox1}) = \hbar v_n T_{DTst}(E,x,F_{ox1}), \quad \Gamma_n^{DTtg}(E,x,F_{ox2}) = \hbar v_n T_{DTtg}(E,x,F_{ox2}) \tag{2.18d}$$

$$\Gamma_n^i(v,p) = 2\,\hbar\, v_n\, p \tag{2.18e}$$

where E_n^{res} is the nth resonance energy level, T_n^{peak} is a peak value at nth resonance energy, Γ_n is the sum of all the partial widths, Γ_n^e is the total elastic width, Γ_n^i is the total inelastic width, Γ_n^{DTst} and Γ_n^{DTtg} are the partial elastic width of the resonant level, v_n is the attempt frequency of the nth resonant level, and p is the probability for a carrier approaching the trapping state to be scattered into the lower state. The widths of the resonance are a function of the applied voltage, and are explicitly affected by the sheet trap density. The formula for the resonant tunneling current density is then [Bla00]

$$J_{RES}(E_n^{res},x,F_{ox1},F_{ox2},p) = \frac{qm_{ox}}{2\pi^2\hbar^3}\sum_{n=1}^{N_{res}} \int_0^{E_{fs}} (E_{fs}-E)\cdot T_n^{tot}(E,x,F_{ox1},F_{ox2},p)\,dE \tag{2.19}$$

where N_{res} is the number of resonant energy levels. On integrating, the current density is given by

$$J_{RES}(E_n^{res},x,F_{ox1},F_{ox2},p) = \frac{qm_{ox}}{2\pi^2\hbar^3}\sum_{n=1}^{N_{res}} \frac{\Gamma_n^{DTst}\Gamma_n^{DTtg}}{\Gamma_n^{DTst}+\Gamma_n^{DTtg}} \times$$

$$\left\{2\left(E_{fs}-E_n^{res}\right)\left[\tan^{-1}\left(\frac{2(E_{fs}-E_n^{res})}{\Gamma_n}\right)+\tan^{-1}\left(\frac{2E_n^{res}}{\Gamma_n}\right)\right]-\frac{\Gamma_n}{2}\ln\left[\frac{(E_{fs}-E_n^{res})^2+\Gamma_n^2/4}{(E_n^{res})^2+\Gamma_n^2/4}\right]\right\} \tag{2.20}$$

Within the resonant tunneling current region, $(E_{fs}-E_n^{res}) \gg \Gamma_n$ and $E_n^{res} \gg \Gamma_n$, and the current density is then approximated by

$$J_{RES}(E_n^{res}, x, F_{ox1}, F_{ox2}, p) \approx \frac{q m_{ox}}{\pi \hbar^3} \sum_{n=1}^{N_{res}} \frac{\Gamma_n^{DTst}\Gamma_n^{DTtg}}{\Gamma_n^{DTst} + \Gamma_n^{DTtg}} \left(E_{fs} - E_n^{res}\right) \tag{2.21}$$

This formula compares directly to the ITAT current density, Equation (16), and shows that the total current density is expressed as the summation of the resonant tunneling components of resonant energy levels.

2.4 Experimental Verification

We illustrate how the characterization and modeling procedure can be applied to devices featuring ultrathin oxides for the purpose of validating the leakage tunneling current model using C-V, I-V, and noise measurements.

2.4.1 Characterization of Ultrathin Oxides

MOS capacitors were fabricated using a manufacturable remote plasma nitrided oxide (RPNO) process [Hat96, Nic00]. About 1.7–4.3 *nm* of gate oxide was grown with both furnace and rapid-thermal based processes. Nitridation was performed at room-temperature by exposing the gate oxide to a short, high-density, remote helicon-based nitrogen discharge. This was then followed by post-nitridation annealing in an inert or low partial-pressure oxygen ambient. MOS capacitors were fabricated with standard processing techniques on both p and n-Si substrate with n^+ and p^+ poly-Si gates, using LOCOS isolation to define the active regions. Following N_2-plasma nitridation and post-nitridation anneal of the gate oxide, a 270 *nm* undoped poly-Si gate layer was deposited. For n^+ gates, P was implanted (5.0×10^{15} cm^{-2}, 45 keV). Activation was performed with a

850 ℃ / 30 min anneal. For p$^+$ gates, the poly-Si was implanted with different doses of B (1.5×10^{15}-4.5×10^{15} cm^{-2}) at 10 keV energy in three of the four quadrants. Rapid-thermal annealing was then performed at 1000 ℃ in N_2 for different durations.

Figure 2.2 depicts a schematic energy band diagram that was simulated by running the program, SCHRED_2.0. This illustrates a n$^+$ polysilicon-SiO_2-p-Si MOS structure in inversion showing the quantization effects of the substrate electron energy. E_c is the Si conduction band edge and E_{fs} is the Fermi level in the Si substrate. E_{ij} is the energy level of the *j*th subband in the *i*th valley, and 79.1% and 16.6% are the carrier occupancy for each energy subband in each valley of *E-k* space.

QM and polysilicon effects induce significant modifications in the CV characteristics, modeling, and parameter extraction procedure [Cle00, Dmo97, Omu00]. For accurate determination of the gate oxide thickness and interface trap density, all these effects have to be taken into account. Assuming that most electrons occupy the ground state of the subband, we can employ the following approximate expression for the total capacitance C_{total}.

$$\frac{1}{C_{total}}=\frac{1}{C_{ox}}+\frac{1}{C_{si}}+\frac{1}{C_{poly}} \tag{2.22}$$

with

$$\frac{1}{C_{si}}=\frac{kT}{q|Q_s(\psi_s)|}+\frac{C_0 z_{av}}{\varepsilon_{si}} \tag{2.23a}$$

$$\frac{1}{C_{poly}}=-\frac{dV_{poly}}{dQ_s}=\frac{dV_{poly}}{dQ_{poly}}=\frac{Q_{poly}}{\varepsilon_{si}qN_{poly}} \tag{2.23b}$$

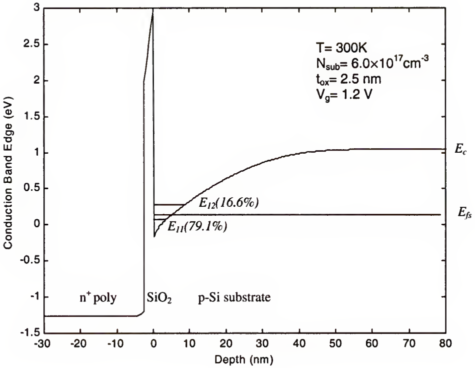


Figure 2.2 Schematic band diagram of a n$^+$ polysilicon-SiO$_2$-p-Si MOS structure showing the quantization effects of the substrate electron energy

$$z_{av} = 3\left(\frac{48\pi^2 m^* q^2}{\varepsilon_{si} h^2}\right)^{-1/3}\left(N_{dep} + \frac{11}{32}\cdot\frac{|Q_s(\psi_s)|}{q}\right)^{-1/3} \tag{2.23c}$$

where C_{ox} is the oxide capacitance, C_{si} is the silicon capacitance, C_{poly} is the capacitance of the polysilicon depletion region, V_{poly} is the voltage drop in the polysilicon depletion region, ψ_s is the surface potential, N_{poly} is the doping concentration in the polysilicon gate, N_{dep} is the depletion charge density, C_0 is a constant, z_{av} is the centroid position of mobile carriers in the inversion or accumulation layer, and m^* is the effective electron mass. For convenience, we can use the following approximate semi-classical expression for $Q_s(\psi_s)$ [Omu00].

$$Q_s(\psi_s) = \frac{\sqrt{2}\varepsilon_{si}kT}{qL_D} F\left(\frac{q\psi_s}{kT}\right) - qN_{dep} \tag{2.24}$$

with

$$N_{dep} = \sqrt{2q\varepsilon_{si}N_{sub}\psi_s} \tag{2.25a}$$

$$F\left(\frac{q\psi_s}{kT}\right) = \sqrt{\left[\exp\left(-\frac{q\psi_s}{kT}\right) + \frac{q\psi_s}{kT} - 1\right] + \left(\frac{n_i}{N_{sub}}\right)^2 \left[\exp\left(\frac{q\psi_s}{kT}\right) - \frac{q\psi_s}{kT} - 1\right]} \tag{2.25b}$$

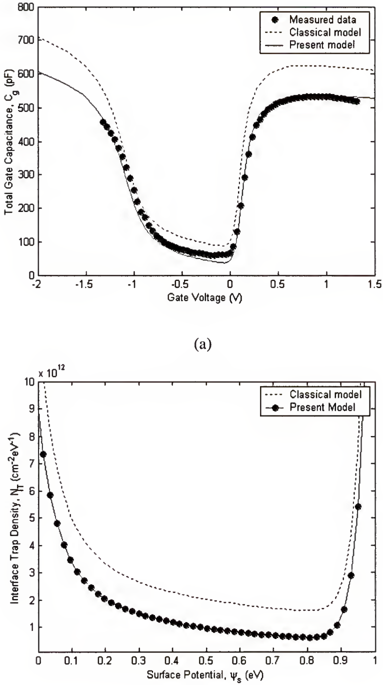
where L_D is the Debye length and $F(q\psi_s/kT)$ is a semi-classical function of the surface potential. In Equation (2.23a), C_0 is introduced to make a correction of effective width of the inversion layer. From self-consistent simulation results for C_0 [Omu00], an empirical and useful expression can be obtained for the (100) silicon surface as

$$C_0 = 0.41 + \exp\left[-\left(\frac{|Q_s(\psi_s)|}{qN_m}\right)^{1/2}\right] \tag{2.26}$$

where N_m is a constant ($=1.264\times10^{11}$ cm^{-2}). The gate voltage applied to polysilicon-SiO_2-p-Si MOS structure is described by

$$V_g = V_{FB} + V_{poly} + \psi_s - \frac{Q_s}{C_{ox}} \tag{2.27}$$

The interface trap density is evaluated from the quasi-static C-V technique. Because the interface trap capacitance C_{it} is in parallel with the silicon capacitance, the following equation is used for extracting the interface trap density N_{it} ($\text{cm}^{-2}\text{eV}^{-1}$).



(a)

(b)

Figure 2.3 Comparison of C-V and interface trap density evaluated by the proposed model, classical model, and measured data. (a) C-V characteristics and (b) evaluation of interface trap density for n$^+$poly-Si nMOSFET with t_{SiON} = 3.21 nm ($t_{ox,eq}$ = 2.2 nm), ε_{SiON} = 5.7ε_0, N_{sub} = 6.0×10^{17} cm^{-3}, N_{poly} = 1.85×10^{20} cm^{-3}, and A_g = 140×70×4 μm^2 at T = 300 K

$$\frac{1}{C_{total,m}}=\frac{1}{C_{ox}}+\frac{1}{C_{si}+C_{it}}+\frac{1}{C_{poly}} \tag{2.28}$$

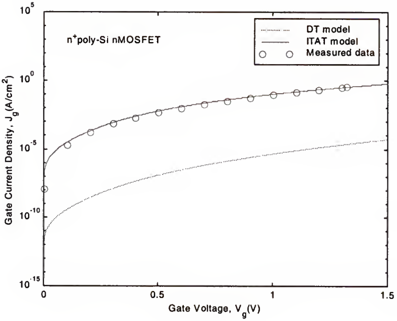
where $C_{total,m}$ is the measured total capacitance and C_{si} is the semi-quantum-mechanical semiconductor surface capacitance including the inversion layer capacitance. The interface trap density is derived from Equation (2.28) as follows

$$N_{it}(\psi_s)=\frac{C_{it}(\psi_s)}{q}=\frac{1}{q}\left[\frac{C_{tatal,m}C_{ax}C_{poly}}{C_{ox}C_{poly}-C_{tatal,m}C_{poly}-C_{total,m}C_{ox}}-C_{si}(\psi_s)\right] \tag{2.29}$$

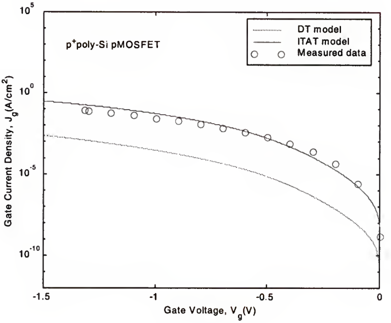
In order to verify the proposed model, the simulation results of the C-V characteristics by using Equations (2.22)–(2.23) is shown in Figure 2.3 (a) with the classical simulation results and the measured data for n$^+$poly-Si nMOSFET. The equivalent oxide thickness $t_{ox,eq}$ can be calculated as $t_{ox,eq}=(\varepsilon_{ox}/\varepsilon_{SiON})\ t_{SiON}$ [Vog98], where the nitrided oxide and oxide dielectric constant, ε_{SiON} and ε_{ox}, are assumed to be 5.7 ε_0 and 3.9 ε_0, respectively. The C-V characteristics simulated by the proposed model agree well with the measured data. Figure 2.3 (b) shows the interface trap density evaluated by using Equation (2.29) and the classical model. Near the band edge, the difference between two models increases drastically. Consequently, when the quantum mechanical influence and the polysilicon depletion effect are anticipated to be significant, the classical model cannot be applied to extract the interface trap density from C-V measured data.

2.4.2 Current-Voltage Characteristics

The gate leakage I-V characteristics were simulated using the proposed ITAT model of Equation (2.16). The I-V characteristics are dependent on the unknown trap density $N_{trap}(x,E)$. It is assumed in our calculation that $N_{trap}(x,E)$ is a constant and equals the interface trap density N_{it}, irrespective of the position and the energy level. Figure 2.4 (a) shows the calculated I-V characteristics of the ITAT model as a function of the gate voltage with the energy loss during ITAT process as a fitting parameter. This result is compared with the direct tunneling model and measured data for n^+poly-Si nMOSFET. In order to corroborate the simulation results, we used the values of the oxide thickness and trap density obtained from C-V evaluation including the QM and polysilicon depletion effect. The simulation was carried out with $t_{SiON} = 3.21\text{nm}$ ($t_{ox,eq} = 2.2\text{nm}$), $\phi_{b,SiON} = 2.6\text{eV}$ [Vog98], $m_{ox} = 0.4m_0$ [Yeo00], $\sigma_t = 5.0\times10^{-14}\text{cm}^2$ [Ghe00b], $N_{trap} = 2.0\times10^{12}\ \text{cm}^{-2}$, $x_t = 0.46\ t_{SiON}$, $\phi_t = 2.5\text{eV}$, and $\lambda = 0.6$ [Yeo00]. From the comparison of the experimental results and ITAT theory, it was found that the energy loss ranges from 0.1 to 0.6 eV for gate voltages 0.3 – 1.5 V. It is shown that the results calculated by ITAT have better agreement with the experimental results than those from the direct tunneling model. This is due to the fact that the direct tunneling effect gives a small contribution to the total tunneling current. With appropriate changes of barrier height, effective mass, and voltage polarity, the models are equally applicable to p-channel MOSFETs. The simulation was performed by using, t_{SiON}=3.21nm ($t_{ox,eq}$=2.2nm), $\phi_{b,SiON}$=2.5eV, $m_{ox}=0.32m_0$, $\sigma_t=5.0\times10^{-14}\text{cm}^2$, $N_{trap}=2.0\times10^{12}\text{cm}^{-2}$, $x_t=0.29t_{SiON}$, ϕ_t=2.4eV, and λ=0.4. Again good agreement between the measured data and simulation results can be observed in Figure 2.4 (b). Figure 2.5 illustrates the effect of trap-related parameters, i.e., trap position located away from the Si-SiO$_2$ interface and trap energy level measured from the conduction band edge of the oxide, on the I-V characteristics for n^+ ploy-Si nMOSFET. The current peaks for traps located in the middle of the oxide layer and

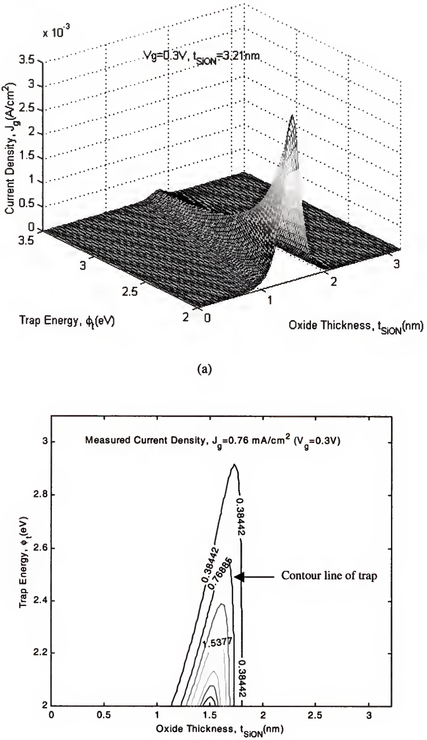


(a)



(b)

Figure 2.4 Comparison of I-V characteristics simulated by the proposed model and DT model, and measured data with (a) t_{SiON} = 3.21nm, ε_{SiON} = 5.7ε_0, $\phi_{b,SiON}$ = 2.6eV, m_{ox} = 0.4m_0, σ_t = 5×10^{-14}cm^2, N_{trap} = 2×10^{12}cm^{-2}, λ = 0.6 (b) t_{SiON} = 3.21nm, ε_{SiON} = 5.7ε_0, $\phi_{b,SiON}$ = 2.5 eV, m_{ox} = 0.32m_0, σ_t = 5×10^{-14}cm^2, N_{trap} = 2×10^{12} cm^{-2}, λ = 0.4



(a)

(b)

Figure 2.5 Illustration of the effect of trap-related parameters on I-V characteristics for n^+poly-Si nMOSFET (a) Influence of trap energy levels and trap positions on current density (b) contour plot matching with experimental data

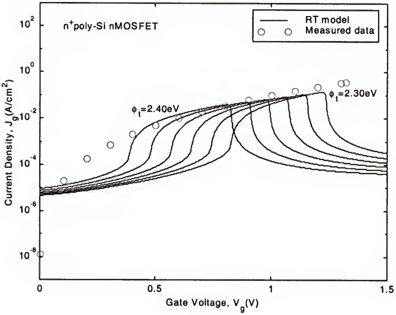


Figure 2.6 Comparison of I-V characteristics calculated by the measured data and the proposed resonant tunneling (RT) model with $v_n = 10^{14}\ \mathrm{s}^{-1}$, $p = 0.01$, $t_{SiON} = 3.21\mathrm{nm}$, $x_t = 0.27t_{SiON}$, $m_{ox} = 0.4m_0$, $\sigma_t = 5\times10^{-14}\ \mathrm{cm}^2$, $N_{trap} = 2\times10^{12}\ \mathrm{cm}^{-2}$

exponentially decreases for traps away from the center of the oxide and at deeper energy levels, as shown in Figure 2.5 (a). Figure 2.5 (b) shows the contour plot of current density matching with experimental results. The trap position $x_t = 0.46\ t_{SiON}$ and energy level ϕ_t=2.5eV extracted from a fitting procedure are consistent with the contour line of trap.

For the purpose of understanding the ITAT process at the microscopic level, we have calculated the resonant tunneling (RT) current for several resonant trap energy levels, as shown in Figure 2.6. For our calculations, we take for the attempt frequency v_n $=10^{14}\ \mathrm{s}^{-1}$ [Ric98] . The RT current curves for resonant energy levels are characterized by the negative differential resistance (NDR) region between the peak and valley. The peak current occurs when the energy of an electron tunneling through the oxide exactly

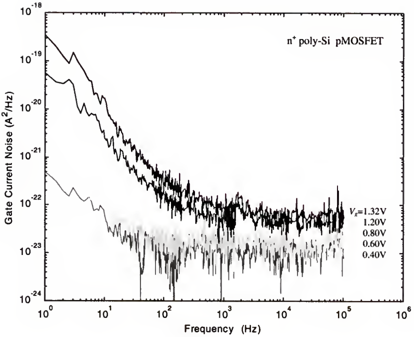


Figure 2.7 Gate current noise spectral density for n$^+$poly-Si nMOSFET with t_{SiON} = 3.21nm ($t_{ox,eq}$ = 2.2nm), N_{sub} = 6.0×10^{17}cm^{-3}, N_{poly} = 1.85×10^{20}cm^{-3}, and A_g = 140×70×4 μm^2 at T=300K

corresponds to the trap energy level. Quantitatively, it is found that the ITAT current can be reproduced by the summation of the resonant tunneling components, based on a theoretical model which takes into account two features, the trap states serving as quantum wells and trapped electrons undergoing inelastic events. This confirms that the ITAT mechanism is probably at the origin of the gate leakage current in ultrathin nitrided oxide MOSFETs.

2.4.3 Leakage Current Noise Characteristics

Figure 2.7 shows a typical gate current noise spectrum measured at low voltages for n$^+$ poly-Si nMOSFET with ultrathin oxide fabricated by remote plasma nitrided oxide (RPNO) process. The noise spectrum clearly shows a $1/f^{\gamma}$ frequency dependence with different power factors γ depending on the gate bias. The magnitudes and power factors of the low frequency current noise are practically a constant between 0.4V and 0.8V. However, when the gate voltage is above 0.8V, the magnitudes and power factors of the low frequency noise increase with an increase in gate voltage. The bias dependence of the $1/f^\gamma$ noise indicates the existence of inelastic processes occurring in the trap states. Moreover, this is in accordance with the dependence of energy loss on the gate voltage. Physically, the $1/f^\gamma$ noise observed at low frequencies implies the existence of slow processes with long relaxation times in the oxide barrier. Electron-phonon scattering involved in this process gives rise to low frequency dissipation in the conductance of the oxide traps. This in turn results in barrier height fluctuation, and cause the fluctuation in the tunneling current.

2.5 Conclusion

A physical model and analysis applicable to the low voltage gate leakage charge transport in ultrathin gate nitrided oxide MOSFETs was presented. The model is based on inelastic trap-assisted tunneling (ITAT) mechanism combined with a semi-empirical direct tunneling current model. The model includes the effect of charge stored in the trap states and the dependence of the energy loss on the oxide field during tunneling through the trap states. It was found that the results simulated by the ITAT model show good agreement with the experimental results. To clarify the mechanisms of the ITAT current based on a collective approach, resonant tunneling (RT) through barriers containing defect state potential wells was formulated. From the comparison of the ITAT model and RT formulation, it was found that the origin of the gate leakage current might be attributed to the ITAT mechanisms in ultrathin nitrided oxide MOSFETs. Furthermore, the ITAT process assumption is supported by the low frequency excess noise spectra.

For the purpose of validating the leakage tunneling current model, the oxide thickness and the interface trap density of gate oxide were determined by the quasi-static C-V method, taking quantum mechanical effects and polysilicon depletion into account . The C-V characteristics simulated by our model agree well with the measured data.

CHAPTER 3
NOISE MODEL OF GATE LEAKAGE CURRENT

3.1 Introduction

One of the important problems associated with the downscaling of CMOS technologies is an increase in the importance of random noise, which is always a practical limit to the performance of a device [Cel99, Sim99]. As a result, the signal-to-noise ratio of analog circuits is reduced, and bit errors occur in data transmission systems. Especially, the scaling of device dimensions, resulting in the use of thinner oxide layers, is necessary for enhancing circuit speed at low voltages, providing the same capacitance within a smaller area, and offering lower programming voltages for non-volatile memory.

It is generally accepted now that the miniaturization of devices will cause an increase of low frequency noise level due to an observed scaling law [Cel99]. Since low frequency noise is strongly technology sensitive, which in some cases can also be used as a predictive or diagnostic tool for device lifetime and reliability issues, the introduction of new processing steps may introduce low frequency components not presently observed or described by existing noise theories [Sim99]. Moreover, the low frequency noise not only determines the lower end of the dynamic range of device operation in the base band, but also has potentially a major impact on the phase noise of nonlinear circuits in the GHz region through up-conversion [Klu00]. In addition to the channel current, gate leakage current in ultrathin gate oxide MOS devices should be considered as a low frequency noise source [Mom98]. It is known that the appearance of noise in the gate current of

MOS structures potentially precedes oxide breakdown [Cru00a, Cru00b, Ner95]. The gate tunneling current noise interpreted at a microscopic scale can be a powerful characterization tool in evaluating the ultrathin oxide reliability [Ner95]. However, if we can understand the physical origin of the noise, we can develop strategies for minimizing it or its influence. Therefore, an accurate modeling and characterization of noise in deep-submicron MOSFETs with ultrathin gate oxide is needed to design future CMOS devices, analog circuits, and new device processing technologies.

In this Chapter, we will present a detailed study of a physics-based compact noise model for deep-submicron MOSFETs with ultrathin gate oxide. In Section 3.2, on the basis of the gate oxide current leakage mechanisms, we employ a barrier height fluctuation model and a Lorentzian-modulated shot noise model of the gate leakage current to explain the excess noise. The excess noise can be interpreted as the sum of $1/f^{\gamma}$ noise and enhanced shot noise. The $1/f^{\gamma}$ noise component at low frequencies is described by thermal noise of the frequency-dependent conductance of the oxide slow traps which modulates the current tunneling through the oxide barrier. The positive correlation between tunneling current components, associated with generation-recombination (G-R) process due to oxide fast traps, produces the Lorentzian-modulated shot noise at higher frequencies, leading to enhanced shot noise. In Section 3.3, we show experimental results, exhibiting the excess noise consisting of $1/f^{\gamma}$ component at low frequencies and enhanced shot noise at higher frequencies. For experimental verification, the proposed noise model is compared with experimental results, and excellent agreement is observed. Finally, Section 3.4 presents some conclusions.

3.2 Formulation of Noise Model

We present an analytical noise model for the gate leakage current through a SiO_2 barrier in the inelastic trap-assisted tunneling regime. Trap-related processes are the most likely cause of excess current noise because traps in the oxide can result in low frequency dissipation in the conductance of oxides and produce the Lorentzian-modulated shot noise associated with generation-recombination (G-R) process at higher frequencies [Ale96, Che99, Ghi87, Kum77]. The gate current noise spectral density consists of two or three Lorentzians in addition to shot noise and $1/f^{\gamma}$ noise.

$$S_I(f) = 2qI \cdot F + \frac{A}{f^{\gamma}} + \sum_i \frac{B_i}{1 + 4\pi^2 f^2 \tau_i^2} \tag{3.1}$$

where the first term corresponds to shot noise with the Fano factor F, the second to flicker noise or $1/f^{\gamma}$ noise, and the third to G-R noise of discrete time constants τ_i. As shown in Figure 3.1, one possible mechanism for $1/f^{\gamma}$ noise contribution is for traps to affect locally the barrier height or shape due to thermal noise of the frequency-dependent conductance of the oxide slow traps [Ghi87, Ian00, Kle82]. This fluctuation in turn modulates the tunneling transmission, and causes the fluctuation in the tunneling current. The mechanism for shot noise associated with G-R process can be explained by carrier transport based on ITAT [Ian00, Lee02]. The generation rate, i.e., the transition rate from the substrate and the gate to the unoccupied trap in the oxide, and recombination rate, i.e., the transition rate from the occupied trap to the substrate and the gate, are caused by the statistical occupancy fluctuation of fast traps in the oxide.

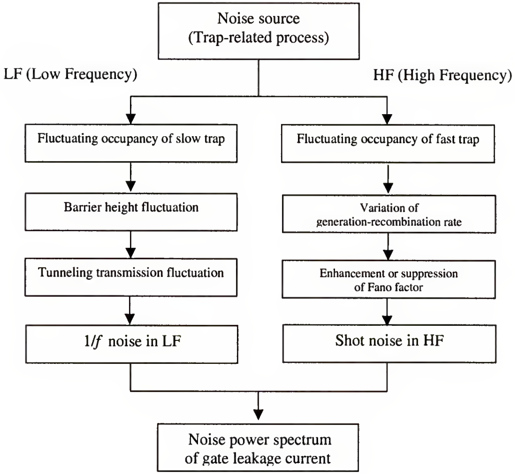

Noise source
(Trap-related process)
LF (Low Frequency)
HF (High Frequency)
Fluctuating occupancy of slow trap
Fluctuating occupancy of fast trap
Barrier height fluctuation
Variation of generation-recombination rate
Tunneling transmission fluctuation
Enhancement or suppression of Fano factor
1/f noise in LF
Shot noise in HF
Noise power spectrum of gate leakage current

Figure 3.1 Flow diagram of the physics-based processes for the noise model calculations in the low and high frequencies

The fluctuations in the generation and recombination rates in turn modulate the tunneling current through traps in the oxide, as illustrated in Figure 3.1. From the trap-assisted tunneling associated with G-R process, therefore, we can obtain an expression consisting of full shot noise and G-R noise, which is referred to as the Lorentzian-modulated shot noise [Vli81]. The observed enhancement of noise at higher frequencies is probably due to G-R noise contributed by some positive correlation [Ian97, Ian98, Rek99, Rek00, Vas02].

3.2.1 Barrier Height Fluctuation Model

The noise equivalent circuit of an ultrathin oxide MOSFET with the source and drain tied together is described in Figure 3.2 [Eat72, Oga97, Vik95, Vog00]. $G_{t,dc}$ is the frequency-independent dc tunneling conductance, R_i is the inversion layer resistance, $G_p(f)$ is the frequency-dependent parallel conductance of oxide traps in $\Omega^{-1}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$, and $C_p(f)$ is the frequency-dependent parallel capacitance of oxide traps in Fcm^{-2}. The $1/f^{\gamma}$ noise might be originated by thermal noise, $4kTG_p(f)$, due to the frequency-dependent parallel conductance $G_p(f)$, producing the barrier height fluctuation. In terms of $G_p(f)/w$ loss observed at low frequencies, the slow traps contributing to the low frequency plateau in $G_p(f)/w$ are responsible for the measured $1/f^{\gamma}$ noise [Ghi87, Kum77, Kir89, Nic67a, Nic67b, Ure89, Ure95].

On the basis of the Wentzel-Kramers-Brillouin (WKB) approximation, the tunneling transmission coefficient for electrons can be expressed as [Dep95]

$$T_t(\phi_b) = \exp\left[-\frac{\sqrt{8m_{ox}}}{\hbar} \int_0^{x_1} \sqrt{\phi_b + E_{fs} - E + \frac{m_\perp}{m_{ox}} E_\perp - q\frac{V_{ox}}{t_{ox}} x} \; dx \right] \tag{3.2}$$

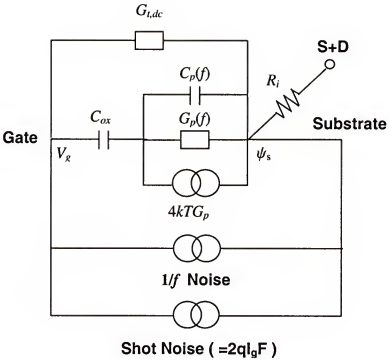


Figure 3.2 Noise equivalent circuit of an ultrathin oxide MOSFET with the source and drain tied together, corresponding to the oxide trap occupancy controlled by semiconductor electrons.

where the classical turning point x_l for direct tunneling is equal to t_{ox}. Due to thermal noise of the equivalent conductance modeling oxide trap occupancy fluctuations, the barrier height ϕ_b fluctuates as follows

$$\phi_b(x,t) = \phi_b + \delta\phi_b(x,t) \tag{3.3}$$

where $\delta\phi_b$ is a small fluctuation in $\phi_b(x,t)$ which is a function of position x and time t. The fluctuation in the tunneling transmission is given by

$$\delta T_t(x,t) = \frac{\partial T_t}{\partial \phi_b} \cdot \delta\phi_b(x,t) \tag{3.4}$$

Using Equations (3.2), (3.3), and (3.4), we can obtain the fluctuations in the tunneling transmission T_t as follows [Kle78, Kle82]

$$\delta T_t(t) = -T_t \cdot \frac{\sqrt{2m_{ox}}}{\hbar} \int_0^{x_1} \frac{\delta\phi_b(x,t)}{\sqrt{\phi_b + E_{fs} - E + \frac{m_\perp}{m_{ox}} E_\perp - q\frac{V_{ox}}{t_{ox}} x}} dx \tag{3.5}$$

Replacing $x_1 = t_{ox}$ for direct tunneling and making a Fourier transform, we find the spectral noise density of the transmission to be

$$S_{T_t}(f) = T_t^2 \cdot \frac{2m_{ox}}{\hbar^2} \times$$

$$\int_0^{t_{ox}} \int_0^{t_{ox}} \frac{S_{\phi_b}(x',x'',f)}{\sqrt{\left(\phi_b + E_{fs} - E + \frac{m_\perp}{m_{ox}} E_\perp - q\frac{V_{ox}}{t_{ox}} x'\right)\left(\phi_b + E_{fs} - E + \frac{m_\perp}{m_{ox}} E_\perp - q\frac{V_{ox}}{t_{ox}} x''\right)}} dx' dx'' \tag{3.6}$$

where $S_{\phi_b}(x',x'',f)$ is the spectral cross-correlation density in thermal noise at positions x' and x'', and is given by [Kle78, Kle82, Kum77, Vik95]

$$S_{\phi_b}(x',x'',f) = \int_0^{x'} \int_0^{x''} \frac{4kTq^2}{A_g t_{ox}} \cdot \mathrm{Re}[Z(f)] \cdot \left[\delta(x_a - x_b) - \frac{1}{t_{ox}}\right] dx_a dx_b \tag{3.7a}$$

with

$$\mathrm{Re}[Z(f)] = \frac{1}{2\pi f} \cdot \frac{\frac{G_p(f)}{2\pi f}}{\left[\frac{G_p(f)}{2\pi f}\right]^2 + [C_{ox} + C_p(f)]^2} \tag{3.7b}$$

where k is Boltzmann's constant, T is the temperature, C_{ox} is the oxide capacitance in F·cm^{-2}, δ is the Dirac delta function, and Re[$Z(f)$] is the real part of frequency-dependent impedance between $x = 0$ and $x = t_{ox}$ in Figure 3.2. Using Equations (3.6) and (3.7), the spectral noise density for the tunneling transmission is found to be

$$S_{T_t}(f) = T_t^2 \cdot \frac{4m_{ox}kTq^2}{\pi\hbar^2 A_g t_{ox}} \cdot \frac{1}{f} \cdot \frac{\dfrac{G_p(f)}{2\pi f}}{\left[\dfrac{G_p(f)}{2\pi f}\right]^2 + \left[C_{ox} + C_p(f)\right]^2} \times$$

$$\int_0^{t_{ox}} \int_0^{t_{ox}} \frac{\displaystyle\int_0^{x'} \int_0^{x''} \left[\delta(x_a - x_b) - \frac{1}{t_{ox}}\right] dx_a dx_b}{\sqrt{\left(\phi_b + E_{fs} - E + \dfrac{m_\perp}{m_{ox}} E_\perp - q\dfrac{V_{ox}}{t_{ox}} x'\right)} \sqrt{\left(\phi_b + E_{fs} - E + \dfrac{m_\perp}{m_{ox}} E_\perp - q\dfrac{V_{ox}}{t_{ox}} x''\right)}} dx' dx'' \tag{3.8}$$

On integrating Equation (3.8), we get the spectral noise density as a function of the oxide voltage ($V_{ox} \leq \phi_b$)

$$\frac{S_{T_t}(f)}{T_t^2} = \frac{\dfrac{G_p(f)}{2\pi f}}{\left[\dfrac{G_p(f)}{2\pi f}\right]^2 + \left[C_{ox} + C_p(f)\right]^2} \cdot \frac{1}{f} \cdot A(V_{ox}) \cdot B(V_{ox}) \tag{3.9}$$

with

$$A(V_{ox}) = \frac{16 m_{ox} kTq^2}{9\pi\hbar^2 A_g t_{ox}^2 X_2^4} \tag{3.10a}$$

$$B(V_{ox}) = \sqrt{X_1(X_1 - qV_{ox})}\left[8X_1(X_1 - qV_{ox}) - 3q^2V_{ox}^2\right] - 2\left[2X_1^2(2X_1 - 3qV_{ox}) + q^3V_{ox}^3\right] \tag{3.10b}$$

$$X_1 = \phi_b + E_{fs} - E + \frac{m_\perp}{m_{ox}} E_\perp, \qquad X_2 = q\frac{V_{ox}}{t_{ox}} \tag{3.10c}$$

where $G_p(f)/2\pi f$ and $C_p(f)$ are independent of frequency at low frequencies. The fluctuations in the tunneling current are generated by the transmission fluctuations. Assuming that a single transmission probability applies to all transitions in calculating the tunneling current [Gar83, Vog98], the spectral density of the current fluctuations is given by

$$S_{I_g}^{1/f}(f) = I_g^2 \cdot \left[\frac{d\ln I(T_t)}{d\ln T_t}\right]^2 \cdot \frac{S_{T_t}(f)}{T_t^2} \approx I_g^2 \cdot \frac{S_{T_t}(f)}{T_t^2} \tag{3.11}$$

The oxide traps are not only continuously distributed in energy but are also spatially distributed in the oxide. In the case of direct tunneling of carriers in the conduction or valence band into traps located at some energy and at some distance x away from the interface, the parallel conductance $G_p(f)$ and capacitance $C_p(f)$ are expressed as [Bal78, Ghi87]

$$C_p(f) = q^2 \iint \frac{N_T(E,x)}{1+4\pi^2 f^2 \tau_{slow}^2(E,x)} \left(-\frac{\partial f_{FD}}{\partial E}\right) dE dx \tag{3.12a}$$

$$\frac{G_p(f)}{2\pi f} = 2\pi f q^2 \iint \frac{N_T(E,x)\tau_{slow}(E,x)}{1+4\pi^2 f^2 \tau_{slow}^2(E,x)} \left(-\frac{\partial f_{FD}}{\partial E}\right) dE\, dx \tag{3.12b}$$

where f_{FD} is the Fermi-Dirac function and $N_T(E,x)$ is the energy and space trap density in $eV^{-1}cm^{-3}$. For an inelastic tunneling associated with energy loss due to multiphonon lattice relaxation [Kir89, Lee02, Tew94], the effective slow time constant $\tau_{slow}(E,x)$ in a direct tunneling regime can be expressed under the Taylor's series approximation as follows

$$\tau_{slow}(E,x) = \tau_{slow0}(E)\exp\left[\frac{E}{kT} + \lambda(E,x)\right] \approx \tau_0(E)\cdot\exp(\lambda_t \cdot x) \tag{3.13a}$$

with

$$\tau_0(E) = \tau_{slow0}(E) \cdot \exp\left(\frac{E}{kT}\right) \approx \frac{f_{FD}}{\sigma_t^{slow} v_{th} n_s} \tag{3.13b}$$

$$\lambda(E,x) = \frac{4}{3}\frac{\sqrt{2m_{ox}}}{\hbar} \cdot \frac{\phi_b^{3/2} - (\phi_b - qF_{ox}x)^{3/2}}{qF_{ox}} \approx \frac{2\sqrt{2m_{ox}\phi_b}}{\hbar}\left(1 - \frac{qV_{ox}}{4\phi_b}\right) \cdot x \approx \lambda_t \cdot x \tag{3.13c}$$

where σ_t^{slow} is the capture cross section of slow traps, v_{th} is the thermal velocity, and n_s is the surface electron concentration. Assuming that $N_T(E,x)$ is uniform in energy and in space over a distance d into the oxide and $\tau_0(E)$ is a slowly varying function of energy, Equations (3.12a) and (3.12b) are found to be [Ghi87, Kum77]

$$C_p(f) = \frac{q^2 N_t^{slow}(E_f)}{2\lambda_t d} \times$$

$$\left\{ 2\lambda_t d + \frac{\tan^{-1}[2\pi f \tau_{0m}]}{\pi f \tau_{0m}} - \frac{\tan^{-1}[2\pi f \tau_{0m}\exp(\lambda_t d)]}{\pi f \tau_{0m}\exp(\lambda_t d)} + \ln\left[\frac{1+(2\pi f \tau_{0m})^2}{1+(2\pi f \tau_{0m}\exp(\lambda_t d))^2}\right]\right\} \tag{3.14a}$$

$$\frac{G_p(f)}{2\pi f} = \frac{q^2 N_t^{slow}(E_f)}{2\lambda_t d} \times$$

$$\left\{ 2\tan^{-1}[2\pi f \tau_{0m}\exp(\lambda_t d)] - 2\tan^{-1}[2\pi f \tau_{0m}] + \frac{\ln\left[1+(2\pi f \tau_{0m})^2\right]}{2\pi f \tau_{0m}} - \frac{\ln\left[1+(2\pi f \tau_{0m}\exp(\lambda_t d))^2\right]}{2\pi f \tau_{0m}\exp(\lambda_t d)}\right\}$$

$$\approx \frac{\pi q^2 N_t(E_f)}{2\lambda_t d} = \text{constant} \qquad \text{for } 2\pi f \tau_{0m} << 1 << 2\pi f \tau_{0m}\exp(\lambda_t d) \tag{3.14b}$$

where $N_t^{slow}(E_f) = N_T(E,x) \cdot d$ is the oxide slow trap density per unit of area at the Fermi energy level in $\text{eV}^{-1}\text{cm}^{-2}$, and in strong inversion, $\tau_{0m} = 1/(\sigma_t^{slow} v_{th} n_s) \propto 1/(C_{ox}V_{ox})$ [Tew94].

3.2.2 Lorentzian-Modulated Shot Noise Model

Shot noise is the electrical fluctuation due to discreteness of the charge that provides direct information on the correlation of different current pulses. Full shot noise is expected if the electrons tunneling through the oxide layer show Poisson statistics. The analysis of shot noise is performed by introducing the Fano factor F defined as $F = S_I(f) / (2qI)$, $S_I(f)$ being the spectral density of current fluctuations as a function of frequency f and I the current flowing in device. Shot noise is suppressed ($0 < F < 1$) or enhanced ($F > 1$), depending on correlation introduced in the behavior of carriers. Shot noise suppression is explained by Pauli exclusion and Coulomb interaction acting on each trap [Ian97, Ian00, Vli81]. Coulomb repulsion effectively forbids a second electron to occupy the other state and inhibit tunneling of electrons in a surrounding region, leading to suppressed shot noise. In contrast, as an electron tunneling into the trap from the substrate channel raises the potential energy of trap states, more states are available for successive tunneling events and the probability to tunnel into the trap increases, implying that electrons entering the trap are positively correlated and enhanced shot noise is to be expected [Ian98, Rek99]. In the presence of generation-recombination processes with electron traps, it was found that the potential barrier fluctuations induced by the fluctuating fixed charge by long-range Coulomb interaction are at the origin of shot noise enhancement [Vas02].

We describe a model for noise and transport based on trap-assisted two-step tunneling in a MOS structure, as shown in Figure 3.3. Introducing the generation rate, i.e., the transition rates from the substrate (g_{st}) and from the gate (g_{gt}) to the unoccupied trap, and the recombination rate, i.e., the transition rates from the occupied trap to the substrate (r_{ts}) and to the gate (r_{tg}), the generation and recombination rate can be represented by

$$
\begin{aligned}
g_{st}(\phi_b, x, F_{ox1}) &= q\sigma_t^{fast} N_t^{fost}(x, qF_{ox1}x - \phi_b)[1 - f_t(x, qF_{ox1}x - \phi_b)]\, g(\phi_b, x, F_{ox1}) \\
g_{gt}(\phi_t, t_{ox} - x, F_{ox2}) &= q\sigma_t^{fost} N_t^{fost}(x, qF_{ox1}x - \phi_b)[1 - f_t(x, qF_{ox1}x - \phi_b)]g(\phi_t, t_{ox} - x, F_{ox2}) \\
r_{tg}(\phi_t, t_{ox} - x, F_{ox1,2}) &= q\sigma_t^{fost} N_t^{fost}(x, qF_{ox1}x - \phi_b) f_t(x, qF_{ox1}x - \phi_b)\, r(\phi_t, t_{ox} - x, F_{ox2}) \\
r_{ts}(\phi_b, x, F_{ox1}) &= q\sigma_t^{fost} N_t^{fost}(x, qF_{ox1}x - \phi_b) f_t(x, qF_{ox1}x - \phi_b)\, r(\phi_b, x, F_{ox1})
\end{aligned}
\tag{3.15}
$$

where $g(\phi_b, x, F_{ox1,2})$ and $r(\phi_b, x, F_{ox1,2})$ are the uniform generation and recombination rate, respectively, and $N_t^{fast}(x,E)$ is the oxide fast trap density at a distance x and energy E in $eV^{-1}cm^{-2}$.

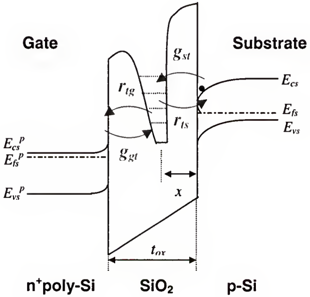


Figure 3.3 Model for Lorentzian-modulated shot noise and transport based on inelastic trap-assisted tunneling in a MOS structure.

The time constant τ_{fast} is associated with the rate equation for carrier number fluctuations ΔN with τ_{fast1} and τ_{fast2} being the time constants related to the variation of the generation-recombination rate due to the carrier number fluctuations through the substrate and gate, respectively. It is assumed that N_t^{fast} and f_t are independent of the number of carriers in the channel per unit area, N. When the carrier flux is one directional, the characteristic time constants around the steady state values are given by

$$\frac{1}{\tau_{fast}(\phi_{b,t}, x, F_{ox1,2})} = \frac{1}{\tau_{fast1}(\phi_b, x, F_{ox1})} + \frac{1}{\tau_{fast2}(\phi_t, t_{ox} - x, F_{ox2})} \tag{3.16a}$$

with

$$\begin{aligned} \frac{1}{\tau_{fast1}(\phi_b, x, F_{ox1})} &= -\left.\frac{dg_{st}(\phi_b, x, F_{ox1})}{dN}\right|_{N=\overline{N}} \\ \frac{1}{\tau_{fast2}(\phi_t, t_{ox} - x, F_{ox2})} &= \left.\frac{dr_{tg}(\phi_t, t_{ox} - x, F_{ox2})}{dN}\right|_{N=\overline{N}} \end{aligned} \tag{3.16b}$$

where $\overline{N}$ is the average number of N. From Equations (2.12),(3.15), and (3.16), we can get the expression

$$\begin{aligned} \frac{1}{\tau_{fast1,2}(\phi_{b,t}, x_{1,2}, F_{ox1,2})} &= \pm q\sigma_t^{fast} N_t^{fast} f_{t1,2} \cdot \left.\frac{\partial a_{1,2}(\phi_{b,t}, x_{1,2}, F_{ox1,2})}{\partial N}\right|_{x_1=x,\, x_2=t_{ox}-x}^{a_1=g,\, a_2=r} \\ &= \pm q\sigma_t^{fast} N_t^{fast} f_{t1,2} \left[\frac{q\partial a_{1,2}(\phi_{b,t}, x_{1,2}, F_{ox1,2})}{\partial \phi_{b,t}} \frac{\partial \phi_{b,t}}{\partial N} + \frac{\partial a_{1,2}(\phi_{b,t}, x_{1,2}, F_{ox1,2})}{\partial F_{ox1,2}} \frac{\partial F_{ox1,2}}{\partial N} \right]_{x_1=x,\, x_2=t_{ox}-x}^{a_1=g,\, a_2=r} \end{aligned} \tag{3.17}$$

where,

$$\left.\frac{\partial a_{1,2}(\phi_{b,t}, x_{1,2}, F_{ox1,2})}{\partial \phi_{b,t}}\right|_{F_{ox1,2}=const} = \frac{a_{1,2}(\phi_{b,t}, x_{1,2}, F_{ox1,2})}{\phi_{b,t}\sqrt{\alpha_{1,2}}\left(1-\sqrt{\alpha_{1,2}}\right)}\times$$

$$\left\{\sqrt{\alpha_{1,2}} + \frac{3B_t\phi_{b,t}^{3/2}\sqrt{\alpha_{1,2}}}{F_{ox1,2}} - 3B_t q x_{1,2}\sqrt{\phi_{b,t}}\left[1-\frac{1}{2}\left(1-\sqrt{\alpha_{1,2}}\right)\right]\right\} \tag{3.18a}$$

$$\left.\frac{\partial a_{1,2}(\phi_{b,t}, x_{1,2}, F_{ox1,2})}{\partial F_{ox1,2}}\right|_{\phi_{b,t}=const} = a_{1,2}(\phi_{b,t}, x_{1,2}, F_{ox1,2})\times$$

$$\left\{-\frac{q x_{1,2}}{\phi_{b,t}\sqrt{\alpha_{1,2}}\left(1-\sqrt{\alpha_{1,2}}\right)} + \frac{2}{F_{ox1,2}} - \frac{3B_t q x_{1,2}\sqrt{\phi_{b,t}}\left(1-\sqrt{\alpha_{1,2}}\right)}{2F_{ox1,2}} + \frac{B_t\phi_{b,t}^{3/2}\beta_{1,2}}{F_{ox1,2}^2}\right\} \tag{3.18b}$$

$$\frac{\partial \phi_{b,t}}{\partial N} \approx \frac{q t_{ox}}{\varepsilon_{ox}}, \qquad \frac{\partial F_{ox1,2}}{\partial N} = -\frac{q}{\varepsilon_{ox}} \tag{3.18c}$$

$$\alpha_{1,2} = \alpha(\phi_{b,t}, x_{1,2}, F_{ox1,2}) = \left[1-\sqrt{1-\gamma_{t1,2}F_{ox1,2}}\right]^2 \tag{3.18d}$$

$$\beta_{1,2} = \beta(\phi_{b,t}, x_{1,2}, F_{ox1,2}) = 1-\left(1-\gamma_{t1,2}F_{ox1,2}\right)^{3/2} \tag{3.18e}$$

$$f_{t1} = 1 - f_t, \qquad f_{t2} = f_t \tag{3.18f}$$

These equations include the effect of charge stored in the trap states on the oxide field during tunneling through the trap states. The transition rates are modulated by the statistical fluctuation of trap occupancy in the oxide. Therefore, the fluctuations in the recombination rate r_{tg} and the generation rate g_{st} around the steady state values are given by

$$\Delta r_{tg}(N,t) = \frac{\Delta N}{\tau_{fost2}} + R(\overline{N},t), \quad \Delta g_{st}(N,t) = \frac{\Delta N}{\tau_{fost1}} + G(\overline{N},t) \tag{3.19}$$

where $\Delta N = N - \overline{N}$, and $R(\overline{N},t)$ and $G(\overline{N},t)$ are the driving noise forces, respectively. It is shown in Equation (3.19) that the recombination and generation rate are decomposed into two contributions where the first term is related to number fluctuations and the second term is due to the full shot noise associated with the random recombination and generation transition, respectively. Making a Fourier analysis of $\Delta r_{tg}(N,t)$ in Equation (3.19) and assuming the correlator for Poissonian current, we can get the noise spectrum for the gate leakage current

$$S_{I_g}^{shot}(f) = S_{I_g}^{Q} + \frac{1}{\tau_{fast2}^{2}(\phi_t, x_2, F_{ox2})} S_{I_g}^{\Delta Q}(f) + \frac{2}{\tau_{fast2}(\phi_t, x_2, F_{ox2})} S_{I_g}^{Q\cdot\Delta Q}(f) \tag{3.20}$$

with

$$S_{I_g}^{Q} = \overline{I_g^{Q} \cdot I_g^{Q*}} = q^2 \overline{S_R(f) \cdot S_R^{*}(f)} = \overline{S_Q(f) \cdot S_Q^{*}(f)} \tag{3.21a}$$

$$S_{I_g}^{\Delta Q}(f) = \overline{I_g^{\Delta Q} \cdot I_g^{\Delta Q*}} = q^2 \overline{S_{\Delta N}(f) \cdot S_{\Delta N}^{*}(f)} = \overline{S_{\Delta Q}(f) \cdot S_{\Delta Q}^{*}(f)} \tag{3.21b}$$

$$S_{I_g}^{Q\cdot\Delta Q}(f) = \overline{I_g^{Q} \cdot I_g^{\Delta Q*}} = q^2\, \overline{\mathrm{Re}[S_R(f) \cdot S_{\Delta N}^{*}(f)]} = \overline{\mathrm{Re}[S_Q(f) \cdot S_{\Delta Q}^{*}(f)]} \tag{3.21c}$$

where Re[ ] denotes the real part of the expression [ ], the asterisk refers to complex conjugate quantities, the superscripts of the noise spectrum *S(f)* are the fluctuating quantities considered, and I_g^{Q} and $I_g^{\Delta Q}$ are the current components due to the total inversion charge, $Q = qN$, and the total inversion charge fluctuation, $\Delta Q = q\Delta N$, respectively. Introducing the charge fluctuations ΔQ around a steady state and using the Langevin equation for ΔQ, we have

$$\frac{d}{dt}\Delta Q+\frac{\Delta Q}{\tau_{fast}(\phi_{b,t},x_{1,2},F_{ox1,2})}=q[G(t)-R(t)] \tag{3.22}$$

Making a Fourier transform and arranging Equation (3.22) with the help of some algebra, we obtain

$$S_{I_g}^{\Delta Q}(f)=\frac{\tau_{fast}^2(\phi_{b,t},x_{1,2},F_{ox1,2})}{1+4\pi^2f^2\tau_{fast}^2(\phi_{b,t},x_{1,2},F_{ox1,2})}\left[S_Q^G(f)+S_Q^R(f)\right] \tag{3.23a}$$

$$S_{I_g}^{Q\cdot\Delta Q}(f)=-\frac{\tau_{fast}(\phi_{b,t},x_{1,2},F_{ox1,2})}{1+4\pi^2f^2\tau_{fast}^2(\phi_{b,t},x_{1,2},F_{ox1,2})}S_Q^R(f) \tag{3.23b}$$

Assuming that $S_Q^G(f)=S_Q^R(f)=2q\overline{I_g}$ and substituting Equations (3.23a) and (3.23b) into Equation (3.20), we can obtain the spectral density of current fluctuations as follows

$$S_{I_g}^{shot}(f)=2q\overline{I_g}\times$$

$$\left[1-\frac{2}{\tau_{fast2}(\phi_t,x_2,F_{ox2})}\frac{\tau_{fast}(\phi_{b,t},x_{1,2},F_{ox1,2})}{1+4\pi^2f^2\tau_{fast}^2(\phi_{b,t},x_{1,2},F_{ox1,2})}+\frac{2}{\tau_{fast2}^2(\phi_t,x_2,F_{ox2})}\frac{\tau_{fast}^2(\phi_{b,t},x_{1,2},F_{ox1,2})}{1+4\pi^2f^2\tau_{fast}^2(\phi_{b,t},x_{1,2},F_{ox1,2})}\right] \tag{3.24}$$

This formula can be either larger or smaller than the full shot noise $2q\overline{I_g}$, depending on the sign of characteristic time constants $\tau_{fast}(\phi_{b,t},x_{1,2},F_{ox1,2})$ and $\tau_{fast2}(\phi_t,x_2,F_{ox2})$. Note that an enhancement in the transition rate occurs when the time constant becomes a negative value, resulting from the positive correlation between current pulses. Physically, the negative time constant means that the change of the carrier flux due to the number fluctuations of carriers decreases [Rek99, Rek00].

3.3. Experimental Verification

Figure 3.4 shows a typical gate current noise spectrum measured at low voltages for n^+ poly-Si nMOSFET with ultrathin nitrided oxide. The noise spectrum clearly shows a $1/f^{\gamma}$ frequency dependence with the power factor $\gamma = 1.0 \sim 2.0$. Gate current noise increased with the increase in gate voltage in the wide range of frequency, while slopes of the frequency dependence deviate from unity with increasing voltage. This implies that more slow trap states are available for trap-assisted tunneling with increasing voltage. The simulation results of the gate current noise spectral density are also shown as a function of frequency for different gate voltages. An excellent agreement between the measurement and simulation at both low and high frequencies is observed. This is attributed to the fact that the noise model is based on the trap-related mechanism, resulting in low frequency dissipation in the conductance of oxide traps and producing the Lorentzian-modulated shot noise associated with G-R processes at higher frequencies.

Figure 3.5 shows the comparison of experimental data and simulation results of the gate leakage current noise at low frequencies. The gate current noise for n^+ poly-Si nMOSFET was measured at room temperature as a function of dc gate current with frequency as parameters, as shown in Figure 3.5 (a). It is observed that there are deviations from I_g^2 scaling at lower current. This implies that the low frequency noise behavior at low voltages is dominated by a shot noise component. At higher current level, however, the simulation results, proportional to I_g^2, are in good agreement with the measured data taken at low frequencies (10 Hz and 50 Hz). This quadratic gate current dependence is expected by the barrier height fluctuation model expressed by Equations (3.9)-(3.11). In order to investigate the behavior of $1/f^{\gamma}$ noise in more detail, the normalized gate current noise as a function of gate voltage at low frequencies is shown in Figure 3.5 (b). The normalized noise power at high voltages is constant as a function of gate voltage, indicating that both the low frequency noise and current are due to the same ITAT process through the oxide barrier.

In Figure 3.6 (a), the measured Fano factor for n^+ poly-Si nMOSFET is plotted as a function of gate voltage for $f = 10$ kHz. It can be noticed that as the gate voltage decreases, the measured Fano factor of nMOSFET at high frequencies reaches a value close to 10^2. For increasing voltages, the Fano factor asymptotically approaches unity. The Fano factor was simulated by the proposed model of Equation (3.24) with $f = 10$ kHz, $t_{SiON} = 3.21$ nm, $\varepsilon_{SiON} = 5.7\varepsilon_0$, $\phi_{b,SiON} = 2.6$eV, $m_{ox} = 0.4m_0$, $N_t^{fast} = 2\times10^{12}$ eV^{-1}cm^{-2}, $x_t = 0.50t_{SiON}$, and $\phi_t = 2.33$eV at $T = 300$K. It is found that the proposed noise model has a good agreement with the experimental results. In order to explain the enhanced shot noise with decreasing voltages, inverse time constants as a function of gate voltage were calculated by using the expressions of Equations (3.17) and (3.18), as shown in Figure 3.6 (b). An enhancement in shot noise occurs as inverse time constants, $1/\tau_{fast1}$ and $1/\tau_{fast2}$, approach the same value with decreasing voltages. By contrast, full shot noise behavior is recovered as the difference between inverse time constants increases. This is due to the positive feedback between trap states and tunneling. When an electron tunneling from the inversion layer to the traps is captured, the potential barrier increases, allowing a decrease of carrier flux (a negative time constant, τ_{fast1}). On the other hand, when a captured electron is emitted from the traps to the gate, the potential barrier decreases, leading to an increase of carrier flux (a positive time constant, τ_{fast2}) and thus an enhanced shot noise [Vas02]. Figure 3.7 illustrates the influence of trap-related

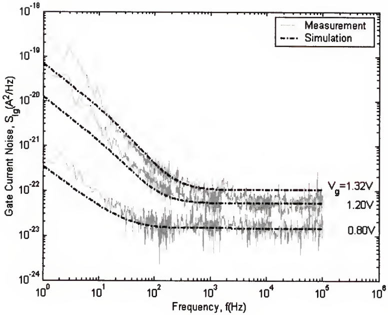
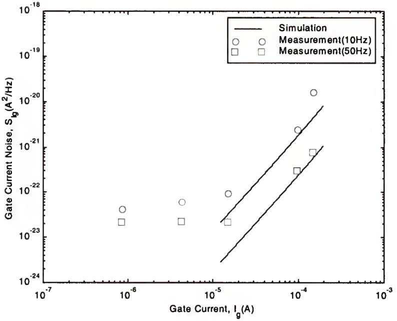
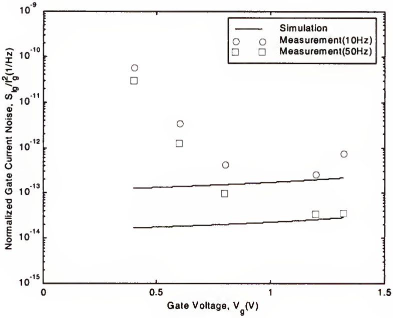


Figure 3.4 Comparison of measured data and simulation results of the gate current noise spectral density as a function of frequency for n$^+$ poly-Si nMOSFET with t_{SiON} = 3.21nm, N_{sub} = 6.0×10^{17}cm^{-3}, N_{poly} = 1.85×10^{20} cm^{-3}, ε_{SiON} = 5.7ε_0, $\phi_{b,SiON}$ = 2.6eV, m_{ox} = 0.4m_0, N_{trap} = 2×10^{12} cm^{-2}, and N_t^{slow} = N_t^{fast} = 2×10^{12} eV^{-1}cm^{-2}at T = 300K.

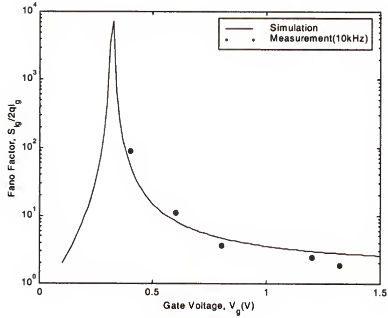


(a)

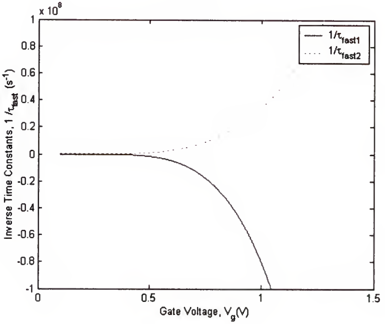


(b)

Figure 3.5 Comparison of measured data and simulation results of (a) gate current noise as a function of gate current and (b) normalized gate current noise as a function of gate voltages at low frequencies for n$^+$ poly-Si nMOSFET with t_{SiON} = 3.21nm, $\varepsilon_{SiON} = 5.7\varepsilon_0$, $\phi_{b,SiON}$ = 2.6eV, $m_{ox} = 0.4m_0$, N_t^{slow}=2×10^{12} eV^{-1} cm^{-2}, $x_t = 0.50t_{SiON}$, and ϕ_t = 2.33eV at T=300K



(a)



(b)

Figure 3.6. Gate bias dependence of (a) Fano factor at $f = 10$ kHz and (b) inverse time constants simulated by the proposed model with t_{SiON} = 3.21nm, N_{sub} = 6.0×10^{17}cm^{-3}, N_{poly} = 1.85×10^{20}cm^{-3}, ε_{SiON} = 5.7ε_0, $\phi_{b,SiON}$ = 2.6eV, m_{ox} = 0.4m_0, and N_t^{fast} = 2×10^{12} eV^{-1}cm^{-2}, x_t = 0.50t_{SiON} , and ϕ_t = 2.33eV at T = 300K.

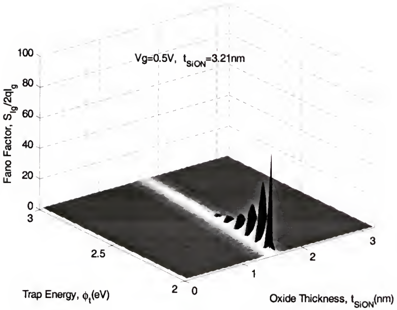


Figure 3.7 Illustration of the influence of trap energy levels and trap positions on Fano factor at f = 10 kHz and V_g = 0.5 V.

parameters on the Fano factor F at $f = 10$ kHz and $V_g = 0.5$ V. The Fano factor peaks for trap located in the middle of the oxide layer, and decreases for traps at deeper energy levels. This is consistent with the trap-dependent current characteristics [Lee02], implying that the shot noise enhancement is due to the trap-assisted tunneling associated with the generation-recombination process.

3.4 Conclusion

A physical and analytical model describing the gate leakage current noise in ultrathin gate oxide MOSFETs was presented. In order to characterize the noise behavior exhibited by the thin nitrided oxide devices, a physics-based noise model of gate leakage current was proposed, which is based on the trap-related tunneling processes. The low and high frequency noise models are based on the barrier height fluctuation model and Lorentzian-modulated shot noise model of the gate leakage current to explain the excess noise behavior, respectively. Slow traps in oxide result in low frequency dissipation in the conductance of oxides, and fast traps produce the Lorentzian modulated shot noise associated with generation-recombination process at higher frequencies. It was verified from the measured data that the newly developed noise model can accurately predict the excess noise behavior of MOS devices with ultrathin gate oxide. In particular, a new formula for the gate leakage current noise is suitable to be implemented in circuit simulators.

CHAPTER 4
DEFECT SPECTROSCOPY USING 1/*f*$^\gamma$ NOISE OF GATE LEAKAGE CURRENT

4.1 Introduction

With the introduction of ultrathin oxides in MOS technologies, the gate leakage current and its associated noise becomes significant even at low frequencies [Lee02, Mom98, Ner95, Sch94b]. This has not only major implications for advanced circuit design but also impacts the experimental study of defects in these advanced structures [Mom98, Nic67b]. It has long been known that the low frequency noise behavior of MOS structure is directly related to trap properties [Cel85, Chr68, Hun90a, Nic67b]. Due to the effects of Si-SiO$_2$ interface trap states on the reliability and quality of MOS structures, its electrical and physical characterization has been a focus of intensive study [Nic67a, Nic82]. However, for ultrathin (<3nm) gate oxides, an accurate and reliable characterization method of the trap properties has not yet emerged [Kon01].

The most frequently used techniques to electrically characterize Si-SiO$_2$ interface are the conductance method [Duv01a, Kon01, Nic67a, Nic82], the C-V method [Cle00, Gre01, Omu00], and the charge pumping method [Mas01]. However, the conductance method loses its resolution due to the large tunneling current in ultrathin gate oxide MOS devices and requires elaborate analysis procedures. In addition, the C-V method needs quantum-mechanical and poly-silicon depletion correction and charge pumping method requires an additional correction for excessive leakage current that can lead to large errors in the extracted trap parameters.

In this Chapter, we will present our attempt to probe the trap properties in MOS device with ultrathin gate oxides by measuring the $1/f^{\gamma}$ low frequency noise of the gate leakage current. Since the $1/f^{\gamma}$ noise depends strongly on the charge fluctuation of the trap states in MOSFETs, information about the trap properties can be extracted from $1/f^{\gamma}$ low frequency noise measurements. There have been several papers on the applications of the $1/f^{\gamma}$ noise technique to determine the trap densities [Cel88, Jay89, Man99, Vil99]. However, all the low frequency noise measurements were performed on the channel current in MOSFETs with relatively thick oxides. Besides the channel current, the gate leakage current should be considered as a low frequency noise source [Lee02, Mon98]. As we will demonstrate, the gate leakage current noise occurring at microscopic level can be a powerful and sensitive tool in evaluating the trap properties in ultrathin gate oxide MOSFETs.

For an accurate and sensitive extraction of trap properties, a new technique is proposed. The basic theory of $1/f^{\gamma}$ noise in terms of complex admittance of the trap states will be presented in Section 4.2. In order to investigate the effects of the spatial trap distribution on the complex admittance and $1/f^{\gamma}$ low frequency noise, analytical expressions are derived for uniform and exponentially decreasing trap distributions in space. After presenting the experimental details in the next section, we will show how the characterization and extraction procedure can be applied to MOS devices featuring ultrathin oxide using the $1/f^{\gamma}$ low frequency noise of the gate leakage current. Trap densities and capture cross sections are accurately determined as a function of trap energy level and trap distance, and the noise characteristics are revealed in terms of the complex admittances of the trap states. Finally, Section 4.5 presents some conclusions.

4.2 $1/f^{\gamma}$ Noise and Admittance Model

An analytical noise model for the gate leakage current through a SiO_2 barrier is presented in the direct tunneling regime. It has been generally accepted that trap-related processes are the major cause of $1/f^{\gamma}$ fluctuations in MOSFETs. The $1/f^{\gamma}$ noise observed at low frequencies might be caused by the fluctuation of the barrier height or shape due to the fact that the frequency-dependent conductance of the oxide traps produces thermal noise resulting in a surface potential fluctuation, as shown in Figure 3.2. This barrier height fluctuation in turn modulates the tunneling transmission, and causes the fluctuations in the tunneling current.

For the extraction of the trap properties, the noise technique may be used by combining the complex MOS admittance of the oxide trap states [Mal71, Saw79]

$$Y_p(f) = G_p(f) + j2\pi f C_p(f) \tag{4.1}$$

Rearranging Equations (3.9) and (3.11) with the help of some algebra, we obtain a calculable expression in terms of the frequency-dependent parallel conductance and capacitance

$$\frac{G_p(f)}{2\pi f} = \frac{1}{2}\left(\frac{I_g^2}{S_{I_g}^{1/f}(f)}\right)\left\{A(V_{ox})B(V_{ox})\frac{1}{f} \pm \sqrt{\left[A(V_{ox})B(V_{ox})\frac{1}{f}\right]^2 - 4\left(\frac{S_{I_g}^{1/f}(f)}{I_g^2}\right)^2 \left[C_{ox} + C_p(f)\right]^2}\right\} \tag{4.2}$$

Provided the noise data over the necessary frequency range in Equation (4.2) are available, the trap information can be obtained from a Cole-Cole plot of the complex admittance in which the frequency loci of $Y_p(f)/2\pi f$ are drawn on the complex $C_p - G_p(f)/2\pi f$ plane. In this plot, the diameter of the arc is equal to the trap density qN_t, and other trap parameters are estimated by the analysis of the detailed geometry of the arc [Mal71, Saw79]. Similarly, using Equations (3.9) and (3.11), and defining $G_p(f)/2\pi f = N_t^{slow}(E_f)\cdot G(f)$ and $C_p(f) = N_t^{slow}(E_f)\cdot C(f)$, we get an analytical expression for the interface trap density

$$N_t^{slow}(E_f) = \frac{1}{2N_1(V_{ox},f)}\left\{-N_2(V_{ox},f) \pm \sqrt{N_2^2(V_{ox},f) - 4N_1(V_{ox},f)N_3(V_{ox},f)}\right\} \tag{4.3}$$

where

$$N_1(V_{ox},f) = \left(\frac{S_{I_g}^{1/f}(f)}{I_g^2}\right)\left[G^2(f) + C^2(f)\right] \tag{4.4a}$$

$$N_2(V_{ox},f) = 2C_{ox}C(f)\left(\frac{S_{I_g}^{1/f}(f)}{I_g^2}\right) - A(V_{ox})B(V_{ox})\frac{1}{f}G(f) \tag{4.4b}$$

$$N_3(V_{ox},f) = \left(\frac{S_{I_g}^{1/f}(f)}{I_g^2}\right)\cdot C_{ox}^2 \tag{4.4c}$$

For an exponentially decreasing trap distribution in space, we consider the form [Bor99]

$$N_T(E,x) = N_T \cdot \exp\left(-\frac{x}{\alpha}\right) \tag{4.5}$$

where α is the characteristic decay depth of the trap density into the oxide. Substituting Equation (4.5) into Equations (3.12a) and (3.12b) and assuming that in most cases α

>10Å, the integral can be approximated analytically. The resulting parallel conductance and capacitance are found to be

$$C_p(f) = \frac{q^2 N_t^{slow}(E_f)}{d\left(\lambda_t + \frac{1}{\alpha}\right)} \left\{ \frac{\tan^{-1}[2\pi f \tau_{0m}]}{2\pi f \tau_{0m}} + (2\pi f \tau_{0m})^{\frac{1}{\alpha\lambda_t}} \cdot \left[\frac{1}{2} \ln\left(1 + (2\pi f \tau_{0m})^2\right) - \ln(2\pi f \tau_{0m}) \right] \right\} \quad (4.6a)$$

$$\frac{G_p(f)}{2\pi f} = \frac{q^2 N_t^{slow}(E_f)}{2d\left(\lambda_t + \frac{1}{\alpha}\right)} \left\{ \frac{\ln\left[1 + (2\pi f \tau_{0m})^2\right]}{2\pi f \tau_{0m}} + (2\pi f \tau_{0m})^{\frac{1}{\alpha\lambda_t}} \cdot \left[\pi - 2\tan^{-1}(2\pi f \tau_{0m})\right] \right\} \quad (4.6b)$$

4.3. Experimental Details

In order to extract the trap properties of the MOS structure, knowledge of the current-voltage and low frequency noise characteristics is required. Prior to the noise measurements, all devices were examined for gate leakage current by measurements of their dc current-voltage characteristics. The low frequency noise measurements were performed for frequencies ranging between 1 Hz and 100 kHz at room temperature. The gate voltage was swept from 0.4 V to 1.32 V. Figure 4.1 shows a typical gate current noise spectrum measured at low voltages for a n^+ poly-Si nMOSFET with ultrathin nitrided oxide. The noise spectrum clearly shows a $1/f^\gamma$ frequency dependence with the power factor $\gamma = 0.9 \sim 1.7$.

For the purpose of validating the proposed method, the conductance measurements are performed using a standard LCR meter. The small signal conductance was measured at different gate biases in the inversion regime, sweeping the signal frequencies from 100 Hz to 1 MHz. For a MOSFET with the source and drain tied

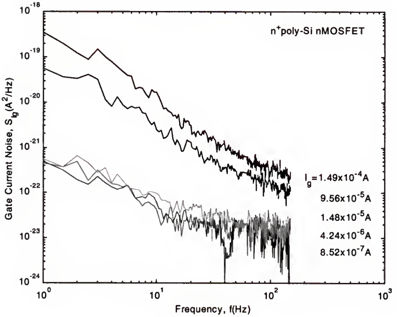


Figure 4.1 Gate current noise spectral density for several current values with $t_{ox,eq}$ = 2.2nm, $N_{sub} = 6.0\times10^{17}\text{cm}^{-3}$, $N_{poly} = 1.85\times10^{20}\,\text{cm}^{-3}$, and $A_g = 140\times70\times4\ \mu\text{m}^2$ at $T = 300\text{K}$

together, measurements were made in the parallel mode, as illustrated in Figure 3.2 [Eat72, Lee02]. From the noise equivalent circuits including the tunneling dc conductance $G_{t,dc}$ and the inversion resistance R_i, the equivalent parallel conductance $G_p(f)/2\pi f$ is related to the measured conductance $G_m(f)$ and capacitance $C_m(f)$ as follows [Eat72, Vog00]

$$\frac{G_p(f)}{2\pi f} = \frac{C_{ox}^2 \dfrac{[G_c(f) - G_{t,dc}(V_g)]}{2\pi f}}{\left[\dfrac{G_c(f)}{2\pi f}\right]^2 + [C_{ox} - C_c(f)]^2} \tag{4.7a}$$

with

$$\frac{G_c(f)}{2\pi f} = \frac{2\pi f \cdot C_m(f) C_c(f) R_i - \dfrac{G_m(f)}{2\pi f}}{G_m(f) R_i - 1} \tag{4.7b}$$

$$C_c(f) = \frac{C_m(f)}{[1 - G_m(f) R_i]^2 + (2\pi f)^2 C_m^2(f) R_i^2} \tag{4.7c}$$

where $G_c(f)$ and $C_c(f)$ are the conductance and capacitance corrected for inversion resistance R_i, respectively. In Equation (4.7a), the dc tunneling conductance $G_{t,dc}(V_g)$ is subtracted from $G_c(f)$ to obtain the ac conductance. $G_{t,dc}(V_g)$ is obtained by differentiating the static gate leakage current curve taken as a function of gate voltages.

4.4 Extraction Procedure and Results

The shape of the low frequency noise spectrum is strongly dependent on the trap distribution in the oxide. Actually, although traps are distributed over space x into the oxide as well as in energy E over the band gap, a complete characterization of traps in the (x, E) window is extremely difficult. It is widely accepted that trap states are classified by two distinct groups. The first is 'fast states' with capture cross sections of about 10^{-16} cm^2, and the second is 'slow states' characterized by capture cross sections less than about 10^{-16} cm^2 [Kir89]. The slow states play a fundamental role in $1/f$ low frequency noise and are due to defect states extended into the oxide layer. From the tunneling point of view, the effective capture cross section of a slow trap located at a distance x from the interface is reduced by [Kir89, Lee03]

$$\sigma_{eff}(x, E) = \sigma_t^{slow}(E) \cdot \exp[-\lambda_t(V_{ox}) \cdot x] \tag{4.8a}$$

with

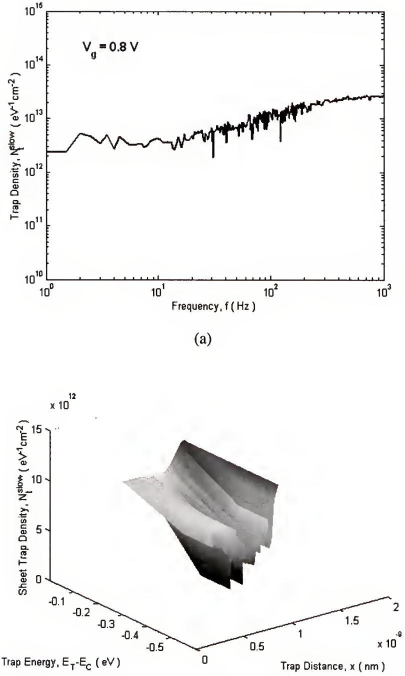
$$\lambda_t(V_{ox}) = \frac{2\sqrt{2m_{ox}\phi_b}}{\hbar}\left(1 - \frac{qV_{ox}}{4\phi_b}\right) \tag{4.8b}$$

In the case of the low frequency noise technique, the tunneling depth x corresponds to a particular measurement signal frequency and is expressed as [Lee03]

$$x = \frac{1}{\lambda_t} \cdot \ln\left(\frac{1}{2\pi f \cdot \tau_0(E)}\right) \tag{4.9}$$

In order to probe the trap energy level, the band gap is scanned by changing the surface potential ψ_s, which is done by varying the gate voltage. Therefore, we can access the (x, E) window of trap states in the oxide, by using frequency and bias-dependent noise measurements. Figure 4.2 (a) shows $N_t^{slow}(f)$ curves as a function of frequency, directly extracted from the measured noise power spectral density using Equations (4.3) and (4.4). This trap spectrum clearly shows the dynamic behavior of oxide trap states in terms of frequencies. $N_t^{slow}(f)$ curves increasing with frequencies reveal a $1/f^{\gamma}$ ($\gamma < 1.0$). The trap densities are plotted as a function of trap energy E and trap distance x, as illustrated in Figure 4.2 (b). The plot clearly visualizes that the slow trap densities estimated near the band edge and at the Si-SiO$_2$ interface are higher than those near the midgap and deeper distance.

Moreover, the gate leakage current noise technique enables the determination of the equivalent parallel conductance of oxide traps at low frequencies. This can be done by using Equation (4.2) and measured noise data. Figure 4.3 (a) shows the conductance loss $G_p(f)/2\pi f$ extracted from the noise measurements for n$^+$ poly-Si nMOSFET.



(a)

(b)

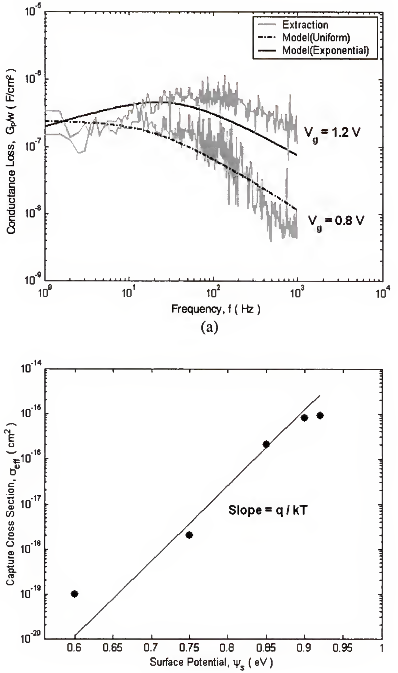
Figure 4.2 Trap density directly extracted from the measured low frequency noise spectra (a) as a function of frequency and (b) trap energy and trap distance.

It was assumed that the trap is uniformly distributed in space for $V_g = 0.8$ V and the trap is exponentially decreasing in space for $V_g = 1.2$ V. The low frequency plateau in the conductance loss is responsible for the $1/f^{\gamma}$ noise and the curvature determines the capture cross sections of the oxide traps [Duv01a, Kir89]. The corresponding capture cross sections are obtained from the extracted conductance loss data and Equation (4.8), and are plotted in Figure 4.3 (b). It is interesting to note that the capture cross sections depend strongly on the surface potential and is nearly an exponential function of the surface potential with a slope of q / kT. The strong energy dependence of the capture cross section of 'slow trap states' observed at low frequencies is in good agreement with the previously published data on conductance spectroscopy techniques [Duv01a, Eat72, Vog00].

The parallel conductance $G_p(f)/2\pi f$ as a function of frequency is measured for different gate voltages. Figure 4.4 (a) shows the parallel conductance obtained by using Equation (4.7) and Figure 3.2. The low frequency plateau extracted from the noise results is confirmed by the conductance measurements. The peak of $G_p(f)/2\pi f$ reduces with decreasing gate voltage and shifts to lower frequency. This is mainly due to the fact that the parallel conductance for lower gate voltage is produced by smaller trap densities and slower time constants of 'fast trap states'. As shown in Figure 4.4 (b), the parallel conductance curves for the uniform trap distribution with the tunneling depth $0.5t_{ox}$ and $0.08\ t_{ox}$ into the oxide are plotted for comparison, respectively. The existence of two distinct traps is verified by the model fitting with the measured data. The fast trap states are at the origin of enhanced or suppressed shot noise associated with the generation-recombination process [Lee02].

For the purpose of investigating the dependency of trap parameters on the complex admittance of oxide traps, the Cole-Cole plots for different trap profiles are calculated using the theoretical model. Figure 4.5 (a) and Figure 4.5 (b) illustrate the shape of the Cole-Cole plots of the trap states admittance for a given frequency range, assuming that the trap density is uniform and exponential decreasing in space, respectively. It can be seen that the arc shape depends strongly on the trap distribution, and that the computed loci for the higher gate voltage have a larger arc diameter and lower peak frequency, giving a direct determination of the trap parameters. From these results, it was shown that a Cole-Cole plot obtained by the measured noise data could yield qualitative information about the trap properties.

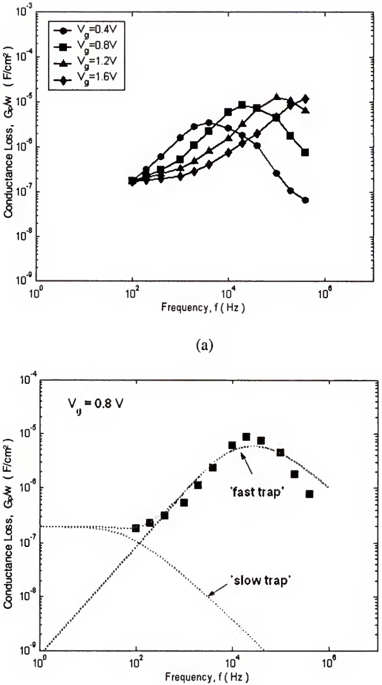
The $1/f^{\gamma}$ noise of MOS structures is given in terms of the complex admittance of trap states, because the noise behavior is directly related to the trap state properties. Therefore, in order to investigate the dependence of trap properties on the low frequency noise in more detail, the Cole-Cole plot on the 2-dimensional $C_p(f)-G_p(f)/2\pi f$ plane can be extended into 3-dimensions. Figure 4.6 (a) shows the frequency loci of the noise in terms of parallel conductance and capacitance in 3 dimensional space, assuming that the trap density is uniform in space. The low frequency noise reduces with increasing frequency, giving a quantitative determination of trap parameters. Curves of Figure 4.6 (b) show the noise power spectrum as a function of conductance for the parameter of frequency. For $V_g = 0.6$V, the noise spectrum becomes independent of frequency at low frequencies, occurring at frequencies much lower than the conductance peak frequency. By contrast, for V_g = 1.32V, the noise spectrum has its highest value around the conductance peak frequency, tending towards a $1/f^{\gamma}$ ($\gamma > 1.0$) type frequency dependence.



(a)

(b)

Figure 4.3 Trap-related parameters extracted from the low frequency noise measurements for n$^+$ poly-Si nMOSFET. (a) Conductance loss $G_p(f)/w$, assuming that the trap is uniformly distributed in space for $V_g = 0.8$ V and the trap is exponentially decreasing in space for $V_g = 1.2$ V and (b) capture cross section of oxide traps. ($t_{ox,eq} = 2.2$ nm, $N_{sub} = 6\times10^{17}\text{cm}^{-3}$, $m_{ox} = 0.4\ m_0$, and $T = 300\text{K}$)



(a)

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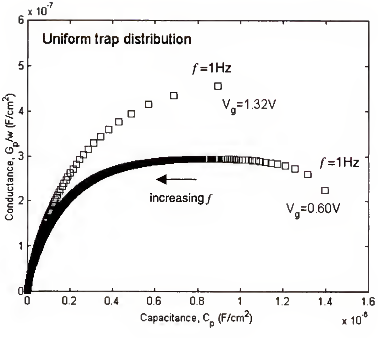
Figure 4.4 Conductance loss characteristics. (a) Measured conductance loss $G_p(f)/w$ as a function of frequency for various gate voltages and (b) theoretical behavior of $G_p(f)/w$ for the slow trap ($d = 0.5\ t_{ox}$) and the fast trap ($d = 0.08\ t_{ox}$), assuming that the trap is uniformly distributed in space.



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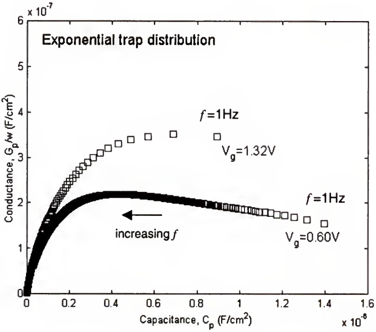
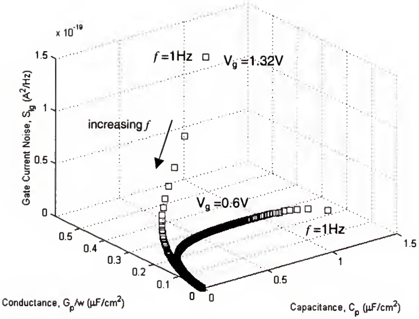
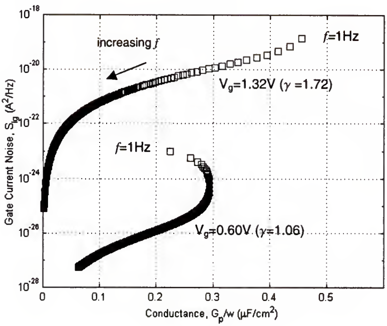


(b)

Figure 4.5 Cole-Cole plots of the trap states admittance calculated from the theoretical model (frequency step Δf = 1 Hz), assuming that (a) the trap density is uniform in space and (b) the trap is exponentially decreasing in space



(a)



(b)

Figure 4.6 Gate current noise characteristics (frequency step $\Delta f = 1$ Hz), (a) as a function of the trap states admittance for a parameter of frequency, and (b) as a function of the conductance loss G_p/w, assuming that the trap density is uniform in space.

As shown in Figure 4.6 (a) and (b), it is apparent that these plots provide a better physical understanding of the low frequency noise source and give information about the trap states responsible for $1/f^{\gamma}$ noise in MOS devices with ultrathin gate oxide.

4.5 Conclusion

The trap state properties of MOS devices with ultrathin oxides were characterized by $1/f^{\gamma}$ low frequency noise of gate leakage current. The trap parameters such as slow trap densities and capture cross section are accurately determined, and the low frequency loci of $1/f^{\gamma}$ low frequency noise are clearly shown by the complex admittance, revealing the dynamic evolution of trap states. It was found that the capture cross sections depend strongly on the surface potential and decrease exponentially with the surface potential towards the midgap. The $1/f^{\gamma}$ noise technique allows the determination of oxide trap densities spectroscopy over the accessible frequency range, and the values near the band edge and the interface are higher than those near the midgap and deeper distance. It was also demonstrated that the parallel conductance spectroscopy can be reproduced by $1/f^{\gamma}$ noise measurements and the Cole-Cole plots can be used to identify the different trap profiling in space. Furthermore, 3-dimensional plots give better insight into the low frequency noise behavior. The results confirm that $1/f^{\gamma}$ noise technique is directly applicable to extract the trap properties in ultrathin oxide MOS devices.

CHAPTER 5
COMPREHENSIVE NOISE PERFORMANCE AT LOW FREQUENCIES

5.1 Introduction

The gate tunneling leakage current resulting from downsizing CMOS technologies is increasingly important in terms of device operation and reliability [Lee01, Mom96, Mom98, Sch94]. As the gate oxide thickness is scaled down to the direct tunneling regime, the tunneling leakage current increases drastically and deteriorates the device performance. Moreover, the current source causes a low frequency noise component which not only determines the lower end of the dynamic range of device operation in the base band, but also has potentially a major impact on the phase noise of nonlinear circuits in the GHz region through up-conversion [Klu00]. Since the impact of the gate leakage current can play a significant role in the overall device characteristics, an exhaustive evaluation of device performance is required over the entire frequency range.

From the noise modeling point of view, the gate leakage current introduces a shot noise current source at high frequencies [Dan95], in addition to the existing channel thermal noise source at the output and induced thermal noise source at the input. The high frequency noise sources are partially correlated, because the MOS transistor can be treated as an RC distributed network meaning that the high frequency gate admittance contains a conductive component [Cap88, Zie86]. At low frequencies, since the gate conductance in ultrathin gate oxide MOSFETs can be substantial due to the oxide traps, it is also observed that a partial correlation between the drain and the gate current noise sources exists. Therefore, in order to accurately predict the noise performance at low frequencies, a physical and rigorous modeling of the correlation effects is required.

The correlation noise measurements at low frequencies have been previously presented for heterojunction bipolar transistors (HBT's) [Bru99, Bru00, Del97, Jar97, Mou01], and the influence of the gate leakage current on the high frequency noise performance was investigated for MESFET's and MODFETs [Puc74, Van92]. To date, no detailed study of low frequency correlation and noise performance with an effect of gate leakage current has been given for ultrathin oxide MOSFETs.

In this Chapter, a comprehensive noise performance at low frequencies is presented, including a physical model of correlation coefficient and its measurements, as well as the minimum noise figure and the optimum source impedance in the presence of a gate leakage current. The correlation coefficient is derived on the basis of the partition noise theory [Rig94, Zie84, Zie87] and the BSIM4 gate leakage current model with the source-drain partition [Cao00], and is compared with correlation noise measurements in terms of the current ratio of the gate to the drain. The analytical expression of low frequency noise performance is newly formulated using the frequency-dependent noise parameters P^{LF}, R^{LF}, and C^{LF}, and the simulation results are graphically presented to investigate how the overall noise performance depends on the gate leakage current and the correlated noise sources at low frequencies. It is confirmed that accurate modeling and understanding of physical noise sources at low frequencies are indispensable for optimum designs of ultrathin oxide MOS devices and circuits.

5.2 Noise Theory

5.2.1 Noise Sources

The high frequency noise behavior of MOSFETs basically arises from the channel thermal noise source at the output, $S_{I_d}^T(f)$, and the induced thermal noise source at the input, $S_{I_g}^T(f)$, as shown in Figure 5.1. These two sources are correlated due to the capacitive coupling, and the corresponding correlation coefficient $C^T(f)$ is complex [Cap98, Dan95, Zie86]. In the low frequency range, the two dominant noise sources at the output are the $1/f^{\gamma}$ noise and the generation-recombination (G-R) noise modeled as follows

$$S_{I_d}^{LF}(f) = 4kT\left[\frac{\rho_d^{1/f}}{f^{\gamma_d}} + \sum_i \frac{\rho_i^{GR}}{1+4\pi^2 f^2 \tau_i^2}\right]\cdot g_{mg}^2 \approx 4kT\cdot\left[\frac{\rho_d^{1/f}}{f^{\gamma_d}}\right]\cdot g_{mg}^2 \qquad (5.1)$$

where k is the Boltzmann constant, T the absolute temperature, $g_{mg} = \partial I_d / \partial V_{gs}$ the transconductance, $\left(\rho_d^{1/f} / f^{\gamma_d}\right)$ the $1/f^{\gamma}$ equivalent input noise resistance, and ρ_i^{GR} and τ_i characterize a G-R noise resistance and a time constant for the ith component, respectively. The physical origins of $1/f^{\gamma}$ noise can be explained by the correlated number and mobility fluctuation model. The correlated model is based on the fact that fluctuations in the occupancy of the oxide traps induce correlated fluctuations in the carrier number and surface mobility [Hun90b]. G-R noise in MOSFETs is caused by random trapping-detrapping of carriers at the defect centers in the depletion region. The G-R noise is usually overshadowed by the higher $1/f^{\gamma}$ surface noise component.

In the case of MOSFETs with ultrathin gate oxide, however, the low frequency noise performance should be modified due to the presence of the gate leakage current I_g,

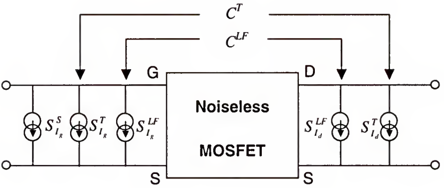


Figure 5.1 Admittance representation of the physical noise sources of ultrathin oxide MOSFET with a gate leakage current noise source

as schematically represented in Figure 5.1. The low frequency noise source at the input, $S^{LF}_{I_g}(f)$, physically follows the same mechanism as observed in the output, and is represented as

$$S^{LF}_{I_g}(f) = 4kT\left[\frac{\rho^{1/f}_g}{f^{\gamma_g}}\right]g^2_g \tag{5.2}$$

where $\left(\rho^{1/f}_g / f^{\gamma_g}\right)$ is the $1/f^{\gamma}$ gate noise resistance and $g_g = \partial I_g / \partial V_{gs}$ is the gate conductance. Note that the low frequency gate noise is proportional to $1/f^{\gamma}$, while the high frequency gate noise shows the quadratic dependence on frequency [Cap88, Zie86]. The low frequency noise sources between the input and the output are partly correlated, and the cross correlation coefficient C^{LF} may not be negligible. The Lorentzian-modulated shot noise source $S^S_{I_g}(f)$ is generated by a trap-assisted tunneling (TAT) through the gate oxide, and can be analyzed by the Fano factor F^{Fano} defined as

$$F^{Fano} = \frac{S_{I_g}^{S}(f)}{2qI_g} \tag{5.3}$$

5.2.2 Noise Models and Correlation Function

In a direct tunneling gate oxide MOSFET, there is a gate leakage current component I_g besides the drain current component I_d. The ratio of gate leakage current to drain current, I_g/I_d, decreases approximately in proportion to the square of channel length, L^2 and typically lies between 1 and 10^{-6}, depending on channel length [Mom96]. As shown in Figure 5.2, the source current I_s is partitioned into I_d flowing to the drain with a partition factor λ, and I_g flowing to the gate with a partition factor $(1-\lambda)$. The average value of the partition factor λ represents the probability that electrons arrive at the drain. Assuming that electrons arriving at the drain or at the gate depend only on the starting point of the electrons in the channel, the drain current noise $S_{I_d}^{LF}(f)$, the gate leakage current noise $S_{I_g}^{LF}(f)$ and the cross noise spectrum $S_{I_dI_g}^{LF}(f)$ at low frequencies are given by [Rig94, Zie84, Zie87]

$$S_{I_d}^{LF}(f) = \left(\frac{1}{1+\lambda_p}\right)^2 \cdot S_{I_s}^{LF}(f) + \left(\frac{1}{1+\lambda_p}\right) \cdot S_{I_g}^{LF}(f) \tag{5.4a}$$

$$S_{I_g}^{LF}(f) = \left(\frac{\lambda_p}{1+\lambda_p}\right)^2 \cdot S_{I_s}^{LF}(f) + \left(\frac{1}{1+\lambda_p}\right) \cdot S_{I_g}^{LF}(f) \tag{5.4b}$$

$$S_{I_dI_g}^{LF}(f) = \frac{\lambda_p}{(1+\lambda_p)^2} \cdot S_{I_s}^{LF}(f) + \left(\frac{1}{1+\lambda_p}\right) \cdot S_{I_g}^{LF}(f) \tag{5.4c}$$

with

$$S_{I_s}^{LF}(f) = \frac{1+\lambda_p}{1-\lambda_p}\left[S_{I_d}^{LF}(f) - S_{I_g}^{LF}(f)\right] \quad \text{and} \quad \lambda_p = \frac{I_g}{I_d} = \frac{1-\lambda}{\lambda} \tag{5.5}$$

where $S_{I_s}^{LF}(f)$ is the source current noise before partitioning into the drain and the gate.

The cross correlation coefficient at low frequencies between the drain and the gate current noise is defined as

$$C^{LF}(f) = \frac{S_{I_d I_g}^{LF}(f)}{\sqrt{S_{I_d}^{LF}(f)\cdot S_{I_g}^{LF}(f)}} \tag{5.6}$$

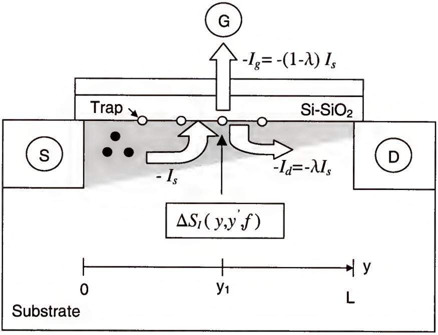


Figure 5.2 Noise current components in ultrathin oxide MOSFET. I_s is partitioned into I_d at the partition factor λ, and I_g at the partition factor $(1-\lambda)$.

Using Equations (5.4a)-(5.4c), (5.5), and (5.6), and rearranging in terms of the ratio of the gate leakage current noise to the drain current noise, $S_{I_g}^{LF}(f)/S_{I_d}^{LF}(f)$, we obtain an expression for the correlation function as follows

$$C^{LF}(f)=\frac{\dfrac{\lambda_p}{(1+\lambda_p)(1-\lambda_p)}\left[1-\dfrac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]+\dfrac{1}{1+\lambda_p}\left[\dfrac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]}{\sqrt{\left\{\begin{array}{l}\dfrac{\lambda_p^2}{(1+\lambda_p)^2(1-\lambda_p)^2}\left[1-\dfrac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]^2+\dfrac{1}{(1+\lambda_p)^2}\left[\dfrac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]^2\\ +\dfrac{(1+\lambda_p^2)}{(1+\lambda_p)^2(1-\lambda_p)}\left[\dfrac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]\left[1-\dfrac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]\end{array}\right\}}} \tag{5.7}$$

For the evaluation of the correlation function at low frequencies, it is necessary to obtain a physical model of $S_{I_g}^{LF}(f)/S_{I_d}^{LF}(f)$, taking the noise generation process into account. Under the assumption that at low frequencies both the drain and gate noise are caused by a random trapping-detrapping of carriers in localized trap states near the Si-SiO$_2$ interface, we can use the Klaassen's formula for the $1/f^{\gamma}$ noise current generator at y and y' along the channel [Kla71]

$$\Delta S_{I_{d,g}}^{LF}(y,y',f)=H^{d,g}(y)\cdot\frac{I^2}{f^{\gamma_{d,g}}g\left(V_i(y)\right)}\delta(y-y') \qquad \text{for} \quad i=0,1 \tag{5.8}$$

where $\delta(y)$ is a delta function, $H(y)$ the local noise source related to a trap efficiency, $g(V_i)$ the channel conductance per unit length at y, $V_0(y)$ the channel voltage at y, and $V_1(y)$ the perturbation voltage induced by the gate leakage current ($V_0(y) \gg V_1(y)$). If the noise source is distributed uniformly over the range $0 < y < y_1$, the noise spectrum ratio may be represented by

$$\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)} = \frac{\frac{1}{L^2}\int_0^{y_1}\int_0^{y_1} H^g(y)\frac{I_g^2}{f^{\gamma_g} g(V_1(y))}\delta(y-y')dydy'}{\frac{1}{L^2}\int_0^{y_1}\int_0^{y_1} H^d(y)\frac{I_d^2}{f^{\gamma_d} g(V_0(y))}\delta(y-y')dydy'} \tag{5.9}$$

where L is the effective channel length. Assuming $H^d(y) = H^g(y)$ and carrying out the integration, bearing in mind that the drain and gate current are respectively [Rao71],

$$I_d = g(V_0(y))\frac{dV_0(y)}{dy} \quad \text{and} \quad I_g = g(V_1(y))\frac{dV_1(y)}{dy} \tag{5.10}$$

yields a simple expression as follows

$$\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)} = \lambda_p \cdot \frac{V_1(y_1)}{V_0(y_1)} \cdot f^{(\gamma_d - \gamma_g)} \tag{5.11}$$

In this formula, the channel voltage $V_0(y)$ as a function of y is given by [Tau98]

$$V_0(y) = \frac{V_{gs} - V_T}{m} - \sqrt{\left(\frac{V_{gs} - V_T}{m}\right)^2 - 2\frac{y}{L}\left(\frac{V_{gs} - V_T}{m}\right)V_{ds} + \frac{y}{L}V_{ds}^2} \tag{5.12}$$

where m is the body-effect coefficient ranging from 1.1 to 1.4, V_T the threshhold voltage, V_{gs} the gate-to-source voltage, and V_{ds} the drain-to-source voltage. According to BSIM4 gate leakage current model including the source-drain partition [Cao00], the perturbation voltage $V_1(y)$ may be rewritten as

$$V_1(y)=\frac{J_{g0}\left\{\left[\exp(-B^*Ky)-1\right]+\frac{y}{L}\left[1-\exp(-B^*Ky)\right]\right\}}{\mu C_{ox}B^{*2}K^2(V_{gs}-V_T-Ky)} \tag{5.13}$$

with

$$B^*=\frac{P_{igcd}t_{ox}B}{V_{gs}^2},\qquad B=\frac{8\pi\sqrt{2qm_{ox}}\phi_b^{3/2}}{3h} \tag{5.14a}$$

$$K=\frac{\left(V_{gs}-V_T-\frac{V_{ds}}{2}\right)\cdot V_{ds}}{\left(V_{gs}-V_T\right)L} \tag{5.14b}$$

where q is the electron charge, ϕ_b the tunneling barrier height, h the Planck constant, t_{ox} the gate oxide thickness, m_{ox} the electron effective mass of the conduction band in the oxide, P_{igcd} a fitting parameter with a default value of 1, μ the mobility, and C_{ox} the gate oxide capacitance per unit area. J_{g0} is the direct tunneling current density with V_{ds}= 0 and is given by [Cao00]

$$J_{g0}=\frac{q^3}{8\pi h\phi_b\varepsilon_{ox}}\cdot C(\phi_b,t_{ox.}F_{ox},V_g)\cdot\exp\left[-\frac{8\pi\sqrt{2m_{ox}}\phi_b^{3/2}[1-(1-|V_{ox}|/\phi_b)^{3/2}]}{3hq|F_{ox}|}\right] \tag{5.15}$$

with a correction function

$$C(\phi_b,t_{ox},F_{ox},V_g)=\exp\left[\frac{20}{\phi_b}\left(\frac{t_{ox}|F_{ox}|-\phi_b}{\phi_{bo}}+1\right)^{\lambda_1}\cdot\left(1-\frac{t_{ox}|F_{ox}|}{\phi_b}\right)\right]\cdot\left(\frac{V_g}{t_{ox}}\right)\cdot N \tag{5.16}$$

where F_{ox} is the electric field in the oxide layer, λ_1 a fitting parameter, ϕ_{bo} the Si-SiO$_2$ barrier height (3.1 eV for electrons and 4.5 eV for holes), and N an indicator of the density of tunneling carriers.

5.2.3 Noise Performance at Low Frequencies

For the calculation of noise performance at low frequencies, the dimensionless noise coefficients P and R are defined as [Puc74].

$$P = \frac{S_{I_d}(f)}{4kT|Y_{21}|} = \frac{1}{4kT|Y_{21}|}\left\{S_{I_d}^{LF}(f) + S_{I_d}^{T}(f)\right\} = P^{LF} + P^{T} \tag{5.17a}$$

$$R = \frac{S_{I_g}^{LF}(f)}{4kTg_g} + \frac{|Y_{21}| \cdot S_{I_g}^{T}(f)}{4kT|Y_{11}|^2} = R^{LF} + R^{T} \tag{5.17b}$$

where $|Y_{21}| \approx g_{mg}$ and $|Y_{11}| \approx 2\pi f C_{gs}$. At low frequencies, R is not due to the capacitive coupling, but due to the trap-assisted tunneling through the gate oxide layer. The gate-to-source capacitance C_{gs} in the linear region and in the saturation region is calculated according to the following formula, respectively

$$C_{gs} = \frac{2}{3}WLC_{ox}\left[1 - \frac{(V_{gd} - V_T)^2}{(V_{gs} + V_{gd} - 2V_T)^2}\right] \quad \text{and} \quad C_{gs} = \frac{2}{3}WLC_{ox} \tag{5.18}$$

where W is the effective channel width and V_{gd} is the gate-to-drain voltage. The cross correlation coefficient $C(f)$ between the drain and the gate can be written as

$$C(f)=\frac{S_{I_dI_g}(f)}{\sqrt{S_{I_d}(f)\cdot S_{I_g}(f)}}=C^{LF}(f)\sqrt{\frac{P^{LF}R^{LF}}{PR}}+C^{T}(f)\sqrt{\frac{P^{T}R^{T}}{PR}} \tag{5.19}$$

With knowledge of the basic noise sources, it is possible to calculate the low frequency noise performance using P^{LF}, R^{LF}, and C^{LF}. We shall consider fundamental noise parameters as a function of the noise spectrum ratio at low frequencies. The minimum noise figure $F_{\min}^{LF}$ can be obtained in terms of the optimum source resistance $R_{s,opt}^{LF}$, the noise resistance r_n^{LF}, the noise conductance g_n^{LF}, and the correlation impedance Z_c^{LF} as follows [Puc74]

$$F_{\min}^{LF}=1+2g_n^{LF}\left(R_c^{LF}+R_{s,opt}^{LF}\right)=1+2g_n^{LF}\left(R_c^{LF}+\sqrt{\left(R_c^{LF}\right)^2+\frac{r_n^{LF}}{g_n^{LF}}}\right) \tag{5.20}$$

with

$$r_n^{LF}=\left(R_g+R_f\right)+\frac{1}{g_{mg}}\frac{\left(\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{4kT}\right)[1-(C^{LF})^2]}{1+\left(\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right)-2C^{LF}\left(\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right)^{1/2}} \tag{5.21a}$$

$$g_n^{LF}=\left(\frac{f}{f_c}\right)^2\cdot\frac{S_{I_d}^{LF}(f)}{4kT}\cdot\left[1+\left(\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right)-2C^{LF}\left(\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right)^{1/2}\right] \tag{5.21b}$$

$$Z_c^{LF}=R_c^{LF}+jX_c^{LF}=\left(R_g+R_f\right)+\frac{1}{j2\pi fC_{gs}}\frac{1-C^{LF}\left(\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right)^{1/2}}{1+\left(\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right)-2C^{LF}\left(\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right)^{1/2}}$$

(5.21c)

where R_g and R_f are the parasitic gate and source resistance, respectively, and f_c is the intrinsic cut-off frequency $(= g_{mg}/2\pi C_{gs})$. For $R_g = R_f = 0$, the minimum noise figure is simplified to the form

$$F_{\min}^{LF} = 1 + \left(\frac{f}{f_c}\right)\cdot\frac{S_{I_d}^{LF}(f)}{2kTg_{mg}}\sqrt{\left[1-(C^{LF})^2\right]\cdot\left[\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]} \tag{5.22}$$

The low frequency noise figure F^{LF} can be written in the form

$$F^{LF} = F_{\min}^{LF} + \frac{g_n^{LF}}{R_s}\left|Z_s - Z_{s,opt}^{LF}\right|^2 \tag{5.23}$$

with

$$Z_{s,opt}^{LF} = \frac{1}{Y_{s,opt}^{LF}} = R_{s,opt}^{LF} + jX_{s,opt}^{LF} = \sqrt{\left(R_c^{LF}\right)^2 + \frac{r_n^{LF}}{g_n^{LF}}} - jX_c^{LF} \tag{5.24}$$

where $Z_s = R_s + jX_s$ is the source impedance, and $Z_{s,opt}^{LF}$ and $Y_{s,opt}^{LF} = G_{s,opt}^{LF} + jB_{s,opt}^{LF}$ are the optimum external source impedance and the optimum source admittance at low frequencies, respectively. From Equations (5.17), (5.21), and (5.24), expressing $Y_{s,opt}^{LF}$ for $R_g = R_f = 0$ in terms of the noise ratio, we can get

$$G_{s,opt}^{LF} = 2\pi fC_{gs}\sqrt{\left[1-(C^{LF})^2\right]\cdot\left[\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]} \tag{5.25a}$$

$$B_{s,opt}^{LF} = -2\pi fC_{gs}\left\{1 - C^{LF}\sqrt{\left[\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]}\right\} \tag{5.25b}$$

In addition to the influence of the correlation on the low frequency noise performance, the shot noise due to the gate leakage current, $S_{I_g}^{s}(f) = 2qI_g F^{Fano}$, has an impact on the noise behavior by modifying the noise parameters, $G_{s,opt}^{LF}$ and $F_{\min}^{LF}$, as follows [Dan95]

$$G_{s,opt}^{LF}\Big|_{leakage} = \sqrt{(2\pi f C_{gs})^2 \left[1-(C^{LF})^2\right] \cdot \left[\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right] + \frac{2qF^{Fano} I_g g_{mg}^2}{S_{I_d}^{LF}(f)}} \tag{5.26a}$$

$$F_{\min}^{LF}\Big|_{leakage} = 1 + \frac{S_{I_d}^{LF}(f)}{2kT}\frac{1}{g_{mg}^2} \cdot G_{s,opt}^{LF}\Big|_{leakage} \tag{5.26b}$$

Using Equations (5.3), (5.25), and (5.26a), the optimum source impedance with the gate leakage current taken into account, $Z_{s,apt}^{LF}\Big|_{leakage} = R_{s,apt}^{LF}\Big|_{leakage} + jX_{s,opt}^{LF}\Big|_{leakage}$, can be rewritten as

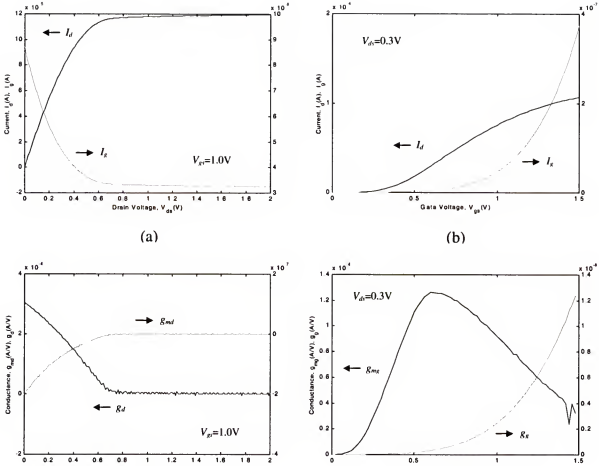
$$R_{s,apt}^{LF}\Big|_{leakage} = \frac{\sqrt{\left(G_{s,opt}^{LF}\right)^2 + \dfrac{2qF^{Fana} I_g g_{mg}^2}{S_{I_d}^{LF}(f)}}}{\left(G_{s,opt}^{LF}\right)^2 + \left(B_{s,opt}^{LF}\right)^2 + \dfrac{2qF^{Fano} I_g g_{mg}^2}{S_{I_d}^{LF}(f)}} \tag{5.27a}$$

$$X_{s,apt}^{LF}\Big|_{leakage} = -\frac{B_{s,apt}^{LF}}{\left(G_{s,opt}^{LF}\right)^2 + \left(B_{s,apt}^{LF}\right)^2 + \dfrac{2qF^{Fano} I_g g_{mg}^2}{S_{I_d}^{LF}(f)}} \tag{5.27b}$$

5.3 Correlation Noise Measurements

Prior to noise correlation measurements, all devices were examined for the drain and gate leakage current by measurements of *I-V* characteristics. Figure 5.3 (a) and (b) illustrate $I_{d,g}$ (V_{ds}) in the strong inversion at V_{gs} = 1.0 V and $I_{d,g}$ (V_{gs}) in the linear region at V_{ds} = 0.3 V, respectively. The gate leakage current in the direct tunneling regime is not negligible, and the ratio of gate current to drain current ranges from ~ 10^{-4} to ~ 10^{-2} V for nMOSFETs with W = 10 μm, L = 10 μm, and t_{ox} = 2.2 nm. A dc analysis of all devices was made including two conductances ($g_g = \partial I_g / \partial V_{gs}$, $g_d = \partial I_d / \partial V_{ds}$) and two transconductances ($g_{mg} = \partial I_d / \partial V_{gs}$, $g_{md} = \partial I_g / \partial V_{ds}$). These parameters are used to obtain the noise equivalent circuit and to extract the cross noise power spectrum. As shown in Figure 5.3 (c) and (d), the transconductance g_{md} has a negative value in the linear region and the lowering of the gate conductance g_g points out the peak of the transconductance g_{mg}.

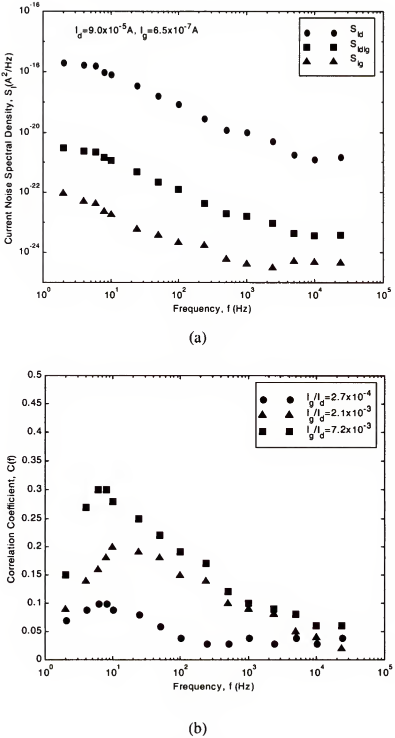
Noise correlation measurements were performed using a HP3582A double channel spectrum analyzer in the frequency range 1 Hz to 25 kHz. Brookdeal 5004 low-noise voltage amplifier were used for both the drain and gate current noise measurement. The voltage noise at the gate and the drain of MOS transistors in a common-source configuration are simultaneously obtained, allowing cross correlation noise acquisition. The drain current noise $S_{I_d}(f)$ and gate current noise $S_{I_g}(f)$ are directly measured at the drain and gate of the device, and the cross noise spectrum $S_{I_d I_g}(f)$ is determined from the cross correlation coefficient and noise measurements. Figure 5.4 (a) shows a typical drain, gate, and their cross noise spectrum measured at $I_d = 9.0\times10^{-5}$ A and $I_g = 6.5\times10^{-7}$ A. The noise spectra clearly show a $1/f^{\gamma}$ frequency dependence with the spectral power factor γ close to unity. As shown in Figure 5.4 (b), we observe that a partial correlation between the drain and the gate current noise sources appears and varies with the current ratio. In the 10 Hz – 1 kHz frequency range, the existence of correlation effects is



(a) (b)

(c) (d)

Figure 5.3 Measured drain and gate current as a function of (a) drain voltage V_{ds} at V_{gs} = 1.0V, (b) gate voltage V_{gs} at V_{ds} = 0.3 V, and measured conductance and transconductance as a function of (c) drain voltage V_{ds} at V_{gs} = 1.0 V, (d) gate voltage V_{gs} at V_{ds} = 0.3 V for nMOSFETs with W = 10 μm, L = 10 μm, and t_{ox} = 2.2 nm



(a)

(b)

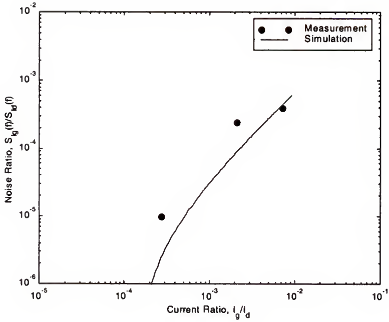
Figure 5.4 Measured correlation noise characteristics (a) Measured drain, gate, and their cross noise spectrum and (b) measured correlation coefficient between drain and gate as a function of frequency f for nMOSFETs with $W = 10\ \mu$m, $L = 10\ \mu$m, and $t_{ox} = 2.2$ nm

probably caused by common noise sources which are slow trap states available for trap-assisted tunneling.

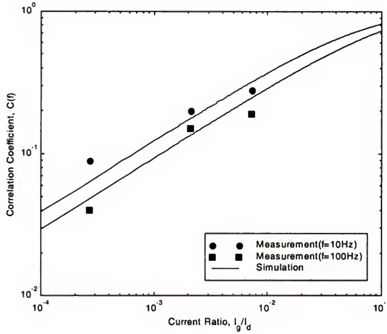
5.4. Simulation Results

5.4.1 Correlation Function Characteristics

The variations of noise ratio $S_{I_g}(f)/S_{I_d}(f)$ and the correlation coefficient $C^{LF}(f)$ with current ratio I_g/I_d are plotted in Figure 5.5 (a) and (b), respectively. These values are compared with those calculated from Equations (5.7) and (5.11) – (5.16) for nMOSFETs biased at $V_{gs} = 0.8$ - 2.0 V and $V_{ds} = 0.3$ V with $W = 10$ μm, $L = 10$ μm, $t_{ox} = 2.2$ nm, $\mu = 300$ cm^2/V-s, $m = 1.2$, $V_T = 0.2$ V, $\phi_b = 3.1$ eV, and $m_{ox} = 0.4$ m_0, and $\gamma_d - \gamma_g = 0.5$. Good agreement is obtained for the noise ratio at $f = 100$ Hz and for the correlation coefficient at $f = 10$ Hz and $f = 100$ Hz. In order to investigate the correlation behavior in more details, the dependencies of the cross correlation coefficient C^{LF} at low frequencies on the current ratio λ_p, the noise ratio $S^{LF}_{I_g}(f)/S^{LF}_{I_d}(f)$, the noise source range y_1/L, and frequency f are shown in Figure 5.6. As illustrated in Figure 5.6 (a), the value of correlation coefficient is reduced as both the current and noise ratio decrease, implying that the correlation coefficient can be negligibly smaller in a device with thicker gate oxide layer. Figure 5.6 (b) indicates that the correlation coefficient depends strongly on the range over which noise is generated and traces the noise source along the channel. This is consistent with the fact that the correlation increases with the stress which produces the percolation leakage path near the drain side [Che01, Jon01]. According to Equations (5.7) and (5.11), the frequency dependence on the correlation coefficient is shown when there is the difference between the drain and the gate frequency power exponent.

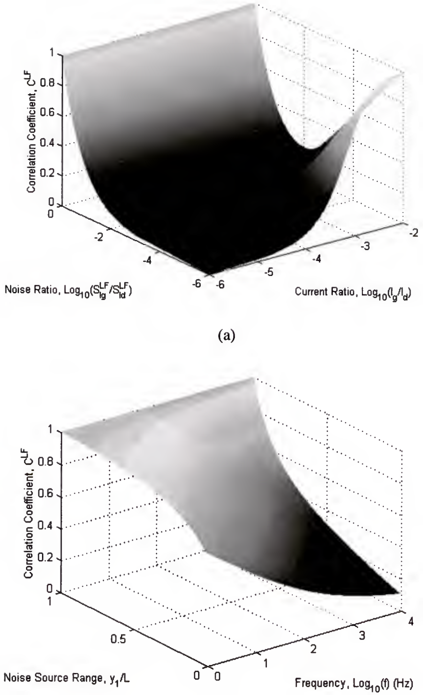


(a)



(b)

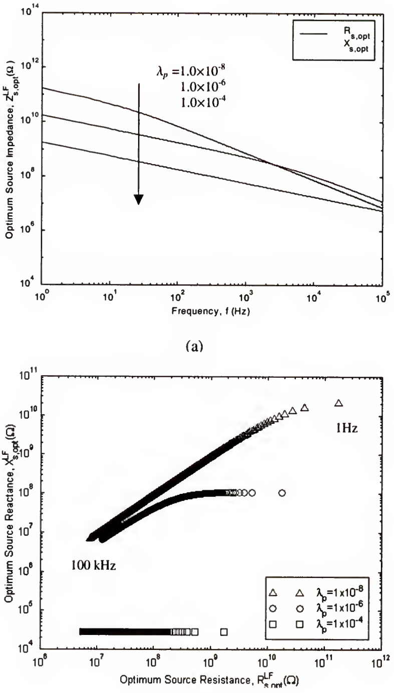
Figure 5.5 Comparison of measured data and simulation results of (a) noise ratio between gate and drain (f = 100 Hz) and (b) correlation coefficient as a function of current ratio I_g/I_d for nMOSFETs biased at V_{gs} = 0.8 - 2.0 V and V_{ds} = 0.3 V with W = 10 μm, L = 10 μm, t_{ox} = 2.2 nm, μ = 300 cm^2/V-s, m = 1.2, V_T = 0.2 V, ϕ_b = 3.1 eV, m_{ox} = 0.4 m_0, and γ_d-γ_g = 0.5



(a)

(b)

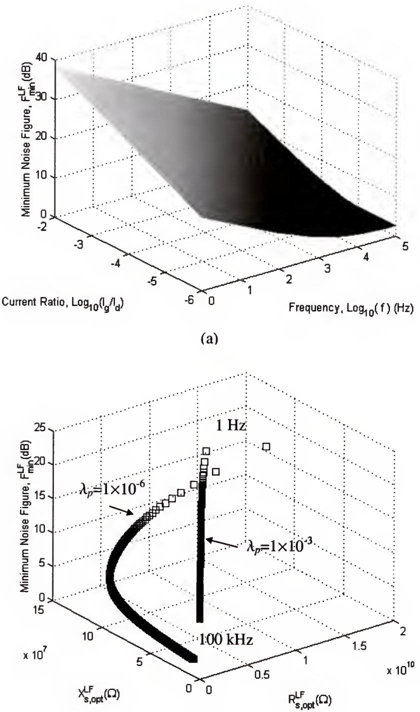
Figure 5.6 Characteristics of the cross correlation function C^{LF}. (a) dependency of C^{LF} on the current ratio and the noise ratio and (b) dependency of C^{LF} on the frequency and the noise source range for nMOSFETs biased at $V_{gs} = 1.0$ V, $V_{ds} = 0.3$ V with $W = 10\ \mu$m, $L = 10\ \mu$m, $t_{ox} = 2.2$ nm, $\mu = 300$ cm^2/V-s, $m = 1.2$, $V_T = 0.2$ V, $\phi_b = 3.1$ eV, and $m_{ox} = 0.4\ m_0$, $\lambda_p = 3.9\times10^{-4}$, $y_1 = 0.01\ L$, and $\gamma_d - \gamma_g = 0.5$



(a)

(b)

Figure 5.7 Optimum source impedance (a) as a function of frequency and (b) as a parameter of frequency for various current ratios in nMOSFETs with $W = 10$ μm, $L = 10$ μm, $t_{ox} = 2.2$ nm, $I_d = 0.1$mA, $g_m = 0.1$ mA/V, $F^{Fano}=1$, $\gamma_d = 1.0$, $\gamma_g = 1.0$, $S_{Id}^{LF} = 1.0\times10^{-16}$ A^2/Hz (@ $f = 1$Hz), m=1.2, y_1=0.01L, and $S_{Ig}/S_{Id} \approx g_g/g_{mg}$



(a)

(b)

Figure 5.8 Characteristics of the minimum noise figure $F_{\min}^{LF}$. (a) dependency of $F_{\min}^{LF}$ on the current ratio and frequency and (b) dependency of $F_{\min}^{LF}$ on the optimum source resistance and reactance for different current ratio in nMOSFETs with $W = 10\ \mu\text{m}$, $L = 10\ \mu\text{m}$, $t_{ox} = 2.2$ nm, $I_d = 0.1$mA, $g_m = 0.1$ mA/V, F^{Fano}=1, γ_d = 1.0, γ_g = 1.0, S_{Id}^{LF} = 1.0×10^{-16} A^2/Hz (@ f = 1Hz), m=1.2, y_l=0.01L, and $S_{Ig}/S_{Id} \approx g_g/g_{mg}$

5.4.2 Noise Performance Characteristics

Figure 5.7 (a) and (b) show how the optimum source impedance varies with the current ratio and frequency. Notice that the optimum source impedance decreases with increasing current ratio and the f^{-1} dependence of the optimum source resistance changes to $f^{-1/2}$ dependence as the gate current becomes larger. Figure 5.8 (a) visualizes the dependencies of the minimum noise figure $F_{\min}^{LF}\big|_{leakage}$ on the gate leakage current and frequency. Observe that the minimum noise figure increases with increasing gate leakage current and clearly exhibits $1/f^{\gamma}$ dependence at low frequencies. As illustrated in Figure 5.8 (b), the variations with the gate leakage current and frequency emphasize the important role played by these parameters in the optimum low frequency noise performance. Therefore, the strong dependence of the minimum noise figure on the current ratio and frequency reflects the importance of minimizing the gate leakage current and noise of ultrathin oxide MOSFETs at low frequencies.

5.5 Conclusion

An analytical model describing the low frequency noise performance in ultrathin gate oxide MOSFETs was presented. For a comprehensive evaluation of noise performance, the model was formulated on the basis of a unified approach involving the gate leakage current and the cross correlation coefficient between the drain and the gate. For the physical modeling of the correlation coefficient at low frequencies, intrinsic noise sources were taken into account, with the help of the partition noise theory and the BSIM4 partition current model. It was found that the correlation behavior is characterized by the current ratio I_g/I_d, the noise source range, and the frequency power factor. The correlation characteristics were verified by correlation noise measurements which can reveal the noise sources distributed along the channel. In addition, in order to investigate the noise performance characteristics at low frequencies, the frequency-dependent noise parameters P^{LF}, R^{LF}, and C^{LF} were introduced and the minimum noise figure, optimum source resistance and reactance were graphically presented. It was shown that the details of low frequency noise performance are modified due to the presence of the gate leakage current and the cross correlation between the input and the output. The results confirmed that the proposed model allows accurate prediction of the noise performance and optimum designs of ultrathin oxide MOS devices at low frequencies. Furthermore, the model is analytically presented in circuit-design oriented form and therefore is suitable to be implemented in circuit simulators.

CHAPTER 6
$1/f^{\gamma}$ NOISE MODEL FOR DRAIN CURRENT

6.1 Introduction

It is widely accept that the shrinkage of MOS devices will cause an increase of the low frequency noise level due to the scaling law [Cel99]. Specifically, the scaling of device dimensions results in the thinning of the oxide layer, leading to excessive gate leakage current [Sch94]. In addition to the channel current, the gate leakage current in ultrathin gate oxide MOS devices should be considered as a low frequency noise source [Mom98].

The existing low frequency noise models are based on the trapping-detrapping of carriers by the tunneling assisted process [Cel85, Chr68, Hun90a, Hun90b] or thermally activated process [Fan91, Sur88]. It was observed from random telegraph signals (RTS) in small MOSFET that switching rates have been thermally activated, often with different activation energies for capture and emission by lattice relaxation [Kir86, Ral84]. Moreover, an inelastic process associated with energy loss during trap-assisted tunneling was proposed to model stress-induced leakage current (SILC) in ultrathin oxides [Lee02, Tak99]. Generally, the low frequency noise behavior is characterized by the trap distribution near the Si-SiO_2 interface. Since traps are distributed over space inside the oxide as well as in energy over the bandgap, the energy and space distribution of trap states should be rigorously modeled [Cel87]. The dissimilar shapes of the energy distribution near the conduction and valence band edge lead to differences in the gate voltage and temperature dependence of the noise observed for n and pMOSFETs [Cha94].

As the channel length and the oxide thickness are shorter and thinner, the effects of the two-dimensional electric field and parasitic resistance on the mobility and *I-V* characteristics become extremely important and have been shown to degrade the transconductance of devices [Ong87, Wu85]. These effects may produce abnormal bias dependence of the low frequency noise behavior [Kol01, Kum00]. For ultrathin oxide MOS devices, the impact of the quadratic mobility degradation factor on the $1/f$ noise was investigated [Mas98]. However, the lack of comprehensive noise models leads to inaccurate prediction of noise performance in advanced MOS devices. In addition, although the process technology can have significant influence on the noise characteristics, a process-dependent noise model has not yet emerged [Hun90a, Hun90b]. Therefore, in order to design future CMOS devices, analog circuits, and new device processing technologies, an accurate modeling and characterization of noise in deep-submicron MOSFETs with ultrathin gate oxide is strongly needed, taking into account effects of the device miniaturization.

In this Chapter, we will present a $1/f^{\gamma}$ drain current noise model for deep-submicron MOSFETs with ultrathin oxide, operating in both the linear and saturation regions. This model incorporates a more realistic trap distribution, and the effects of the two-dimensional electric fields and the parasitic resistance. Physically, the model is based on a tunneling process of carriers between the Si-SiO$_2$ interface and oxide trap states, followed by a thermally activated process due to lattice relaxation. The dependence of the drain current noise on the doping profile is described through the bulk charge parameter.

In Section 6.2, an improved analytical mobility and current model for advanced MOS devices including the parasitic source-drain series resistance is developed with the dependence of the effective field on the doping profile. Section 6.3 deals with an effective time constant model based on the tunneling assisted-thermally activated (TATA) processes. Also, we formulate a new model for trap distribution over energy and space. In this formulation, the trap density inside the bandgap increases as energy becomes close to the conduction and valence band edges, and the trap density versus trap distance is an exponentially decreasing distribution. On the basis of TATA process, a new noise model is formulated by taking the device structure and processes into consideration through a realistic trap distribution, a bulk charge parameter, and parasitic resistance. Moreover, this noise model accounts for the gate-bias dependence of the frequency exponent of the noise power spectrum. In Section 6.4, in order to demonstrate the applicability of the developed model, we illustrate how the device characterization and parameter extraction procedure can be applied to MOS devices featuring short channel length and ultrathin oxide thickness. In Section 6.5, the developed drain current and noise models are compared and verified with experimental results for nMOSFETs. Finally, some conclusions are presented in Section 6.6.

6.2 Mobility and I-V Model

The electron mobility in the surface inversion layer along the channel direction y depends on normal field $E_N(y)$ and lateral field $E_L(y)$ and can be expressed as [Han82, Wu85]

$$\mu_n(y) = \frac{\mu_{n0}}{1+\beta_1|E_N(y)|+\beta_2|E_L(y)|} \tag{6.1a}$$

with

$$\left|E_N(y)\right| = \frac{C_{ox}}{2\varepsilon_{si}}\left[V_{gs}^{'} - V_{FB} - \psi_s - V(y) + \frac{\zeta\left|Q_b(y)\right|}{C_{ox}}\right], \qquad \left|E_L(y)\right| = \left|\frac{dV(y)}{dy}\right| \tag{6.1b}$$

$$Q_b(y) = -\sqrt{2\varepsilon_{si} q N_{sub}\left[V(y) + \psi_s - v_{th}\right]}, \qquad \psi_s = 2v_{th}\ln\left(\frac{N_{sub}}{n_i}\right) \tag{6.1c}$$

where μ_{n0} is the maximum electron mobility in the inversion layer, β_1 is an empirical constant, $\beta_2=\mu_{n0}/v_{sl}$ with the scattering-limited velocity v_{sl}, C_{ox} is the gate oxide capacitance per unit area, ε_{si} is the silicon dielectric permittivity, $V_{gs}^{'}$ is the internal gate-source voltage, V_{FB} is the flat band voltage, ψ_s is the surface inversion potential, $V(y)$ is the potential distribution along the channel, ζ is a bulk charge parameter through which the dependence of the effective field on the doping profile is described [Kru88], $Q_b(y)$ is the silicon bulk charge, N_{sub} is the substrate doping density, n_i is the intrinsic carrier density, $v_{th} = kT/q$ is the thermal voltage, and q is the electron charge. The drain current of nMOSFETs operating in strong inversion is written by [Wu85]

$$I_d = W\mu_n(y)Q_n(y)\frac{dV(y)}{dy} \tag{6.2a}$$

with

$$Q_n(y) = C_{ox}[V_{gs}^{'} - V_T(V_{ds}^{'}) - V(y)] \tag{6.2b}$$

$$V_T(V_{ds}^{'}) = V_{FB} + \psi_s + \zeta\frac{\left|Q_{b,eff}(V_{ds}^{'})\right|}{C_{ox}}, \qquad \left|Q_{b,eff}(V_{ds}^{'})\right| = \frac{1}{V_{ds}^{'}}\int_0^{V_{ds}^{'}}\left|Q_b(V)\right|dV \tag{6.2c}$$

where $Q_n(y)$ is the electron charge density per unit area, W is the effective channel width, and $V_{ds}^{'}$ is the internal drain-source voltage. Putting Equation (6.1c) into Equation (6.2c) and expanding the threshold voltage around $V_{ds}' = 0$, we can obtain

$$V_T(V_{ds}') = V_{T0} - k_{bulk}' V_{ds}'$$

$$= \left[V_{FB} + \psi_s + \frac{\zeta}{C_{ox}} \sqrt{2q\varepsilon_{si} N_{sub}(\psi_s - v_{th})} \right] + \zeta \frac{\sqrt{2q\varepsilon_{si} N_{sub}(\psi_s - v_{th})}}{4(\psi_s - v_{th})C_{ox}} V_{ds}' \tag{6.3}$$

Assuming that the parasitic source and drain resistance are characterized by a resistor R, the relationship between the external voltage (V_{gs}, V_{ds}) and the internal voltage (V_{gs}', V_{ds}') can be written as [Cho92]

$$V_{gs}' = V_{gs} - R \cdot I_d, \qquad V_{ds}' = V_{ds} - 2R \cdot I_d \tag{6.4}$$

Using Equations (6.1)-(6.4) and integrating along the channel length L, the drain current $I_{d,lin}$ for short-channel MOSFETs biased in the linear region is then approximated as [Cho92, Wu85]

$$I_{d,lin} = \frac{W}{L} \mu_{n,eff} C_{ox} \frac{(V_{gs} - V_{T0} - k_{bulk} V_{ds}) V_{ds}}{1 + V_{ds} / E_c L} \tag{6.5a}$$

with

$$\mu_{n,eff} = \frac{\mu_{n0}}{1 + \alpha_1 (V_{gs} - V_{T0} - k_{bulk} V_{ds}) + \alpha_2 (V_{gs} - V_{T0} - k_{bulk} V_{ds})^2} \tag{6.5b}$$

$$E_c = \frac{2 v_{sat}}{\mu_{n,eff}}, \qquad k_{bulk} = \frac{1}{2} - k_{bulk}', \qquad \alpha_1 = \alpha_0 + \frac{W}{L} 2R \mu_{n0} C_{ox} \tag{6.5c}$$

where $\mu_{n,eff}$ is the effective mobility, α_1 and α_2 are the mobility degradation parameters, v_{sat} is the carrier saturation velocity, and E_c is the critical saturation field. Note that

Equation (6.5b) is an analytical effective mobility model which can be applied to ultrathin gate oxide nMOSFETs [Mas98, McL95, Ong87]. In the saturation mode of operation, the lateral electric field reaches the critical field E_c and carriers travel with the saturated velocity v_{sat} near the drain section of the length L_{sat}. Using Equations (6.4) and (6.5a), and considering channel-length shortening effects, the drain current in the saturation region is obtained as [Cho92]

$$I_{d,sat} = \frac{W}{L}\mu_{n,eff}C_{ox}\frac{\left(V_{gs}-V_{T0}-k_{bulk}V_{dsat}\right)V_{dsat}}{\left(1+\frac{V_{dsat}}{E_cL}\right)+\frac{W}{L}\mu_{n,eff}C_{ox}RV_{dsat}-\frac{L_{sat}}{L}} \tag{6.6a}$$

with

$$V_{dsat} = \frac{-\left(V_{gs}-V_{T0}+2k_{bulk}E_cL\right)+\sqrt{\left(V_{gs}-V_{T0}+2k_{bulk}E_cL\right)^2+8k_{bulk}E_cWLC_{ox}Rv_{sat}\left(V_{gs}-V_{T0}\right)}}{4k_{bulk}WC_{ox}Rv_{sat}} \tag{6.6b}$$

$$L_{sat} = l\cdot\ln\left(\frac{\left(V_{ds}-V_{dsat}^{*}+V_0\right)+\sqrt{\left(V_{ds}-V_{dsat}^{*}+V_0\right)^2-\left(V_{dsat}+2RI_{d,sat}-V_{dsat}^{*}+V_0\right)^2+l^2E_c^2}}{lE_c+V_{dsat}+2RI_{d,sat}-V_{dsat}^{*}+V_0}\right) \tag{6.6c}$$

$$V_{dsat}^{*} = V_{gs}-V_{FB}-\psi_s-\frac{V_{gs}-V_{T0}-2k_{bulk}V_{dsat}}{1+WC_{ox}Rv_{sat}} \tag{6.6c}$$

$$l = \sqrt{\frac{\varepsilon_{si}}{C_{ox}}X_j}, \qquad V_0 = \frac{qN_{sub}l^2}{\varepsilon_{si}} \tag{6.6d}$$

where V_{dsat} is the drain saturation voltage and X_j is the drain junction depth.

6.3 Formulation of Noise Model

6.3.1 Effective Time Constant Model

It was found that the capture or emission time constant is energy-activated and could be either enhanced or reduced by the applied gate voltage. The traditional McWhorter's approach based on the tunneling process may have problems on this account [And90, McW57, Tew94]. For ultrathin oxide MOSFETs, we suggest a model based on a tunneling process of carriers, followed by the thermally activated process due to lattice relaxation multiphonon capture-emission in oxide trap states, as shown in Figure 6.1 [Lee02, Tew94]. This is called the tunneling assisted-thermally activated (TATA) model. To model the switching response, we assume that both the capture and emission time constants may be represented by the sum of two time constants, one being tunneling assisted and the other being thermally activated. Specifically, we write

$$\frac{1}{\tau_{c,e}} = \frac{1}{\tau_{th}} + \frac{1}{\tau_{tun}} \tag{6.7}$$

where $\tau_{c,e}$ is a capture or emission time constant. The thermally activated time constant τ_{th} is given by

$$\tau_{th} = \tau_{th0} \exp\left(\frac{E}{kT}\right) = \tau_{th0} \exp(\lambda_{th} E) \tag{6.8}$$

where τ_{th0} is the thermally activated attempt time, E is the activation energy, and λ_{th} is an exponential factor of thermal activation process. From a Taylor's series approximation for the tunneling time constant τ_{tun} in a direct tunneling regime, τ_{tun} can be simplified to [And90, Tew94]

$$\tau_{tun} = \tau_{tun0}\exp[\lambda(E,x)] \approx \tau_{tun0}\exp\left[q\lambda_{tun}\left(1-\frac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\cdot x\right] \tag{6.9a}$$

with

$$\lambda(E,x) = \frac{4}{3}\frac{\sqrt{2m_{ox}}}{\hbar}\cdot\frac{\phi_b^{3/2}-(\phi_b-qF_{ox}x)^{3/2}}{qF_{ox}},\quad \lambda_{tun} = \frac{2\sqrt{2m_{ox}\phi_b}}{q\hbar},\quad F_{ox} \approx \frac{V_{ox}}{t_{ox}} = \frac{V_{gs}-V_{T0}}{t_{ox}} \tag{6.9b}$$

where τ_{tun0} is the tunneling attempt time ($\approx 10^{-10}$ s), λ_{tun} is the exponential factor of tunneling process, t_{ox} is the gate oxide thickness, m_{ox} is the effective mass of tunneling carriers ($0.40m_0$ for electrons and $0.32m_0$ for holes) , ϕ_b is the tunneling barrier height (3.1 eV for electrons and 4.5 eV for holes), $\hbar$ is the reduced Planck constant, F_{ox} is the electric field in the oxide layer, V_{ox} is the oxide voltage, and x is the distance of oxide trap located from the Si-SiO$_2$ interface. Using Equations (6.7), (6.8), and (6.9), the effective time constant can be rearranged in strong inversion as

$$\tau_{c,e}(E,x) = \tau_{c0,e0}(E,x)\cdot\exp\left[\lambda_{th(c,e)}E + q\lambda_{tun(c,e)}\left(1-\frac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\cdot x\right] \tag{6.10}$$

where $\tau_{c0,e0}$ is a capture or emission attempt time constant, $\lambda_{th,c}$ and $\lambda_{th,e}$ are exponential factors of the capture and emission thermal activation process, respectively, and $\lambda_{tun,c}$ and $\lambda_{tun,e}$ are exponential factors of the capture and emission tunneling process, respectively. The rate of the capture-emission process relaxing to an equilibrium state can be defined in terms of its effective time constant τ_{eff} which is given by

$$\tau_{eff}(E,x) = \frac{\tau_c(E,x)\cdot\tau_e(E,x)}{\tau_c(E,x)+\tau_e(E,x)} \approx \tau_{eff0}\cdot\exp\left[\lambda_{th,eff}E + q\lambda_{tun,eff}\left(1-\frac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\cdot x\right] \tag{6.11a}$$

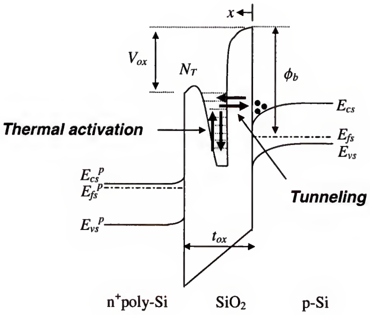


Figure 6.1 Energy band diagram of the tunneling assisted – thermally activated (TATA) process

with

$$\tau_{eff0} \approx \frac{\tau_{c0}(E,x)\cdot\tau_{e0}(E,x)}{\tau_{c0}(E,x)+\tau_{e0}(E,x)}, \quad \lambda_{th,eff} = \lambda_{th,c} + \lambda_{th,e}, \quad \lambda_{tun,eff} = \lambda_{tun,c} + \lambda_{tun,e} \qquad (6.11b)$$

where τ_{eff0} is an effective attempt time constant, and $\lambda_{th,eff}$ and $\lambda_{tun,eff}$ are exponential factors of the thermal activation and tunneling process, respectively.

6.3.2 Trap Distribution Model

A nonuniform trap distribution over a distance in the oxide near the Si-SiO$_2$ interface can also cause a plateau at low frequencies that is similar to generation-recombination noise [Fan86]. Besides nonuniformity in the trap distribution in the oxide, band-bending due to a gate bias, a work function, or oxide charges pulls down the traps, causing the carriers to encounter more traps [Cel87, Sur86]. Therefore, the trap charge distribution is expressed over energy E and distance x in the oxide as follows

$$N_T^i(E,x) = N_{T0} \cdot \exp\left[\xi_1 \left| E - E_i \right| + \left(\xi_2 \frac{V_{gs} - V_{T0}}{t_{ox}} + \xi_3 \right) \cdot x \right] \tag{6.12}$$

where E_i is the intrinsic Fermi level, and ξ_1, ξ_2, and ξ_3 are exponential factors characterizing the distribution of traps in the oxide.

It is worthwhile to consider the practical aspect of trap distribution over energy in a MOS structure. In spite of the fact that Equation (6.12) has the capability of probing the trap distribution, this expression may be insufficient to obtain a reasonable fit to the experimental results. We propose a new model for trap charge distribution over energy at the Si-SiO$_2$ interface. In the new model, the conduction and valence band tail has the form of a sum of two exponentials, respectively

$$N_{Tc}(E) = N_{Tc0}\left[(1-\xi_c) \cdot \exp\left(-\frac{E_c - E}{kT_{c0}} \right) + \xi_c \cdot \exp\left(-\frac{E_c - E}{kT_{c1}} \right) \right] \tag{6.13a}$$

$$N_{Tv}(E) = N_{Tv0}\left[(1-\xi_v) \cdot \exp\left(-\frac{E - E_v}{kT_{v0}} \right) + \xi_v \cdot \exp\left(-\frac{E - E_v}{kT_{v1}} \right) \right] \tag{6.13b}$$

where E_c and E_v are the conduction and valence energy band, respectively, and N_{Tc0}, ξ_c, T_{c0}, and T_{c1} are the trap parameters for the conduction band tail, and N_{Tv0}, ξ_v, T_{v0}, and T_{v1} are the trap parameters for the valence band tail. However, this form results in a complicated formula for the noise spectrum. Simplifying Equations (6.13a) and (6.13b), and including the spatial distribution of traps, we can obtain a more realistic model for the trap charge distribution

$$N_T^{C,V,M}(E,x) = N_{T0}\left[\begin{array}{l}(1-\xi_c)\exp\left(-\dfrac{E_c-E}{kT_c}+\xi_2\dfrac{V_{gs}-V_{T0}}{t_{ox}}x+\xi_3 x\right)\\ +(1-\xi_v)\exp\left(-\dfrac{E-E_v}{kT_v}+\xi_2\dfrac{V_{gs}-V_{T0}}{t_{ox}}x+\xi_3 x\right)+\dfrac{1}{2}(\xi_c+\xi_v)\end{array}\right] \tag{6.14}$$

Figure 6.2 shows the trap density distribution as a function of energy and trap distance from the Si-SiO$_2$ interface. In this figure, the trap density inside the bandgap increases as the energy becomes closer to the conduction and valence band edges due to tailing effects. The trap density versus trap distance is an exponentially decreasing function away from the interface.

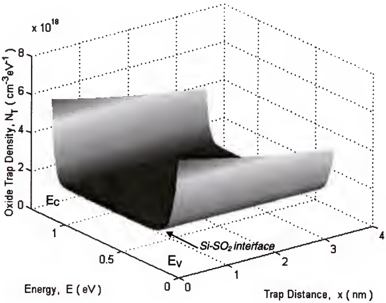


Figure 6.2 Trap density distribution as a function of energy and trap distance from the Si-SiO$_2$ interface. ($V_{gs} = 0.7$ V, $V_{T0} = 0.45$ V, $N_{T0} = 6.25\times10^{18}$ cm^{-13}eV^{-1}, T_c = 300 K, $T_v = 600$ K, $\xi_c = \xi_v = 0.2$, $\xi_2 = 10$ V^{-1}, $\xi_3 = -1.0\times10^{7}$ cm^{-1})

6.3.3 Low Frequency Noise Model

The tunneling assisted-thermally activated (TATA) time constant model may be used to explain $1/f^\gamma$ noise in MOSFETs, where the carriers are assumed to be tunneling to traps located in the oxide layer, and to be followed by a thermal activation process in the oxide trap states. For traps far from the Fermi level, the traps contribute an insignificant amount of noise because most of the time the traps are either empty or filled. Integrating over the noise components of the occupancy of traps within the elemental volume $\Delta x \Delta y \Delta z$, the noise power spectral density due to all the traps in the gate oxide is obtained [Hun90a, Hun90b]

$$S_{\Delta N_T}(f) = \int_{E_v}^{E_c} \int_0^W \int_0^{ox} 4N_T(E,x,y,z) \cdot f_t(1-f_t)\Delta y \cdot \frac{\tau_{eff}(E,x)}{1+4\pi^2 f^2 \tau_{eff}^2(E,x)} \cdot dxdzdE \qquad (6.15)$$

where $N_T(E,x,y,z)$ is the charge density of traps and f_t is the probability that a trap is filled given by the Fermi factor

$$f_t = \frac{1}{1+\exp\left(\dfrac{E-E_{fn}}{kT}\right)} \qquad (6.16)$$

with E the trap energy level and E_{fn} the trap quasi-Fermi level. Note that the term $f_t(1\text{-}f_t)$ is a peaked function about the electron quasi-Fermi level and reflects the fact that only the traps near the electron quasi-Fermi level contribute to fluctuations or noise. Assuming that the energy and spatial distribution of traps is given by Equation (6.12) and $f_t(1\text{-}f_t)$ behaves like a delta function, the integral in Equation (6.15) can be approximated as an analytical expression

$$S_{\Delta N_T}(f) = \frac{\Delta y \cdot W \cdot kT \cdot N_{T0} \exp[\xi_1 |E_{fn} - E_i|]}{q\lambda_{tun,eff}\left(1 - \frac{V_{gs} - V_{T0}}{4\phi_b / q}\right) \cdot \left[2\pi\tau_{eff0} \exp(\lambda_{th,eff} E_{fn})\right]^{(\gamma-1)} \cdot f^{\gamma} \cdot \cos\left[\frac{\pi}{2}(\gamma - 1)\right]} \tag{6.17a}$$

with

$$\gamma = 1 + \frac{\xi_2 (V_{gs} - V_{T0})}{q\lambda_{tun,eff} t_{ox}\left(1 - \frac{V_{gs} - V_{T0}}{4\phi_b / q}\right)} + \frac{\xi_3}{q\lambda_{tun,eff}\left(1 - \frac{V_{gs} - V_{T0}}{4\phi_b / q}\right)} \tag{6.17b}$$

where the slope of the spectrum is directly related to the gate bias.

If we consider a section of channel with width W and length Δy, fluctuations in the trapped oxide charge will induce correlated fluctuations in the channel carrier number and mobility. The resulting fractional change in the local drain current can be represented as [Hun90a, Hun90b]

$$\frac{\Delta I_d}{I_d} = -\left(\frac{1}{\Delta Q_n} \cdot \frac{\delta \Delta Q_n}{\delta \Delta Q_T} \pm \frac{1}{\mu_{eff}} \cdot \frac{\delta \mu_{eff}}{\delta \Delta Q_T}\right) \cdot \delta \Delta Q_T \tag{6.18}$$

where $\Delta Q_n = Q_n W \Delta y$, $\Delta Q_T = Q_T W \Delta y$, and Q_n and Q_T are total charge of channel carriers and occupied traps per unit area. The sign of the mobility term is chosen either positive for acceptor-like traps or negative for donor-like traps. The ratio $R_0 = \delta \Delta Q_n / \delta \Delta Q_T$ in Equation (6.18) describes the efficiency of the drain current modulation corresponding to a variation of the trapped charge. The coefficient R_0 depends on the bias and on the spatial location of the trapping center within the oxide layer and is given by [Pac99]

$$R_0 = \frac{C_{inv}}{\frac{\varepsilon_{ox}}{t_{ox} - x_t} + (C_{dep} + C_{it} + C_{inv})\left(1 + \frac{x_t}{t_{ox} - x_t}\right)} = \frac{t_{ox} - x_t}{t_{ox}} \cdot \frac{Q_n}{Q_n + Q_n^*} \tag{6.19a}$$

with

$$C_{inv} = \frac{q^2}{kT} N_{inv} = \frac{q}{kT} Q_n, \qquad Q_n^* = \frac{kT}{q}\left(C_{ox} + C_{dep} + C_{it}\right) \tag{6.19b}$$

$$x_t = \frac{\ln\left(\dfrac{1}{2\pi f \tau_{eff0}}\right) - \lambda_{th,eff} E}{q\lambda_{tun,eff}\left(1 - \dfrac{V_{gs} - V_{T0}}{4\phi_b / q}\right)} \tag{6.19c}$$

where C_{inv} is the capacitance of the inversion layer, N_{inv} is the areal density of electrons in the inversion layer, C_{dep} is the depletion-layer capacitance, C_{it} is the interface trap capacitance, and the distance of charged trap from the Si-SiO$_2$ interface, x_t, is obtained by rewriting Equation (6.11a) in terms of the characteristic frequency. On the basis of Matthiessen's rule [Jay89], we can readily find that

$$\delta\mu_{eff} = \mu_{eff}^2 S(x_t, N_{inv}) \cdot \frac{\delta\Delta Q_T}{qW\Delta y} \tag{6.20}$$

where $S(x_t,N_{inv})$ is a scattering rate which is a function of the distance x_t of the trapping state [Jay89] and of the carrier density N_{inv} [Hun90c], and is strongly affected by channel quantization [Pac99]. In order to properly account for these effects in ultrathin oxide MOSFETs, we employ an empirical model for the scattering coefficient $S(x_t,N_{inv})$ in a linear approximation as [Jay89, Van00]

$$S(x_t, N_{inv}) = S_1 - S_2 \ln\left(\frac{Q_n}{q}\right) + S_3 \ln\left(\frac{r_{\max}}{x_t}\right) \approx \frac{1}{S_0\sqrt{x_t / r_{\max}} \cdot \sqrt{Q_n}} \tag{6.21}$$

where $r_{\max} \approx (\varepsilon_{ox} + \varepsilon_{si})/(C_{ox} + C_{dep} + C_{it})$ is the maximum distance from the scattering charge for which the effect of image charges can be neglected and S_0 is the scattering constant in cm/C$^{1/2}$Vs. Substituting Equations (6.19) and (6.20) into Equations (6.18), and using Equations (6.2b) and (6.3), the power spectral density of the local current fluctuations is obtained as

$$S_{\Delta I_d}(f) = (\Delta I_d)^2 = \left[\frac{I_d}{Q_n W \Delta y}\left(R_0 \pm S\mu_{eff}\frac{Q_n}{q}\right)\right]^2 \cdot S_{\Delta Q_T}(f) \qquad (6.22a)$$

with

$$Q_n = qN_{inv} = C_{ox}[V_{gs}^{'} - V_{T0} - (1 - k_{bulk}^{'})V(y)] \qquad (6.22b)$$

$$S_{\Delta Q_T}(f) = q^2 \cdot S_{\Delta N_T}(f) \qquad (6.22c)$$

where $S_{\Delta Q_T}(f)$ is the power spectral density of fluctuations in the total charge of occupied traps over the area $W\,\Delta y$. Performing the integration over the channel length, the total noise power spectral density of the drain current is obtained as

$$\begin{aligned} S_{I_d}(f) &= \frac{1}{L^2}\int_0^L S_{\Delta I_d}(y,f)\Delta y\ dy \\ &= \frac{qkT \cdot I_d^2}{WL^2\left(1 - \dfrac{V_{gs} - V_{T0}}{4\phi_b / q}\right)\lambda_{tun,eff}\left[2\pi\tau_{eff0}\exp(\lambda_{th,eff}E_{fn})\right]^{(\gamma-1)} \cdot f^{\gamma} \cdot \cos\left[\dfrac{\pi}{2}(\gamma-1)\right]} \qquad (6.23) \\ &\quad \int_0^L N_{T0}\exp\left[\xi_1\left|E_{fn} - E_i\right|\right] \cdot \frac{1}{Q_n^2}\left(R_0 \pm S\mu_{eff}\frac{Q_n}{q}\right)^2 dy \end{aligned}$$

Combining $k_{bulk} = 0.5 - k_{bulk}^{'}$ and $C_{ox} = \varepsilon_{ox}/t_{ox}$, and replacing the integration over y by integration over Q_n yield

$$S_{I_d}(f) = \frac{qkT \cdot I_d \cdot t_{ox}}{WL^2 \varepsilon_{ox} \left(1 - \frac{V_{gs} - V_{T0}}{4\phi_b / q}\right) \lambda_{tun,eff}(0.5 + k_{bulk}) \cdot \left[2\pi\tau_{eff0} \exp(\lambda_{th,eff} E_{fn})\right]^{(\gamma-1)} \cdot f^{\gamma} \cdot \cos\left[\frac{\pi}{2}(\gamma - 1)\right]}$$

$$\int_{Q_{n2}}^{Q_{n1}} \frac{\mu_{n0} W Q_n - \beta_2 I_d}{1 + \frac{\beta_1 C_{ox}}{\varepsilon_{si}}\left(V_{gs}^{'} - V_{FB} - \psi_s\right) - \frac{\beta_1}{2\varepsilon_{si}} Q_n} \left(N_{TA}^i \frac{R_0^2}{Q_n^2} \pm N_{TB}^i \frac{R_0 S}{Q_n} + N_{TC}^i S^2\right) dQ_n \tag{6.24a}$$

where

$$Q_{n1} = C_{ox}\left(V_{gs} - RI_d - V_{T0}\right) \tag{6.24c}$$

$$Q_{n2} = C_{ox}\left(V_{gs} - RI_d - V_{T0} - (0.5 + k_{bulk})(V_{ds} - 2RI_d)\right) \tag{6.24d}$$

$$N_{TA}^i = N_{T0} \exp\left[\xi_1 \left|E_{fn} - E_i\right|\right] = N_{T0}\left(\frac{N_{sub}}{n_i}\right)^{\xi_1 kT}, \; N_{TB}^i = \pm N_{TA} \frac{2\mu_{eff}}{q}, \; N_{TC}^i = N_{TA} \frac{\mu_{eff}^2}{q^2} \tag{6.24b}$$

Substituting Equations (6.19a) and (6.21) into Equation (6.24a) and integrating, we can get an analytical expression for the drain current noise power in the linear region

$$S_{I_d}^{linear}(f) = \frac{qkT \cdot I_d \cdot t_{ox}}{WL^2 \varepsilon_{ox} \left(1 - \frac{V_{gs} - V_{T0}}{4\phi_b / q}\right) \lambda_{tun,eff}(0.5 + k_{bulk}) \cdot \left[2\pi\tau_{eff0} \exp(\lambda_{th,eff} E_{fn})\right]^{(\gamma-1)} \cdot f^{\gamma} \cdot \cos\left[\frac{\pi}{2}(\gamma - 1)\right]}$$

$$\times \left[N_{TA}^i A^*(V_{gs}, V_{ds}) + N_{TB}^i B^*(V_{gs}, V_{ds}) + N_{TC}^i C^*(V_{gs}, V_{ds})\right] \tag{6.25a}$$

where

$$A^*(V_{gs}, V_{ds}) = \left(\frac{t_{ox} - x_t}{t_{ox}}\right)^2 P \cdot \left\{ \begin{array}{l} \frac{(Q_a - Q_b)}{(Q_a - Q_n^*)^2} \cdot \ln\left[\frac{(Q_a + Q_{n2})(Q_n^* + Q_{n1})}{(Q_a + Q_{n1})(Q_n^* + Q_{n2})}\right] \\ - \frac{(Q_b - Q_n^*)}{(Q_a - Q_n^*)}\left[\frac{1}{(Q_n^* + Q_{n1})} - \frac{1}{(Q_n^* + Q_{n2})}\right] \end{array} \right\} \tag{6.25b}$$

$$B^*(V_{gs},V_{ds}) = \sqrt{\frac{r_{\max}}{x_t}}\left(\frac{t_{ox}-x_t}{t_{ox}}\right)\frac{P}{S_0}\frac{2}{\left(Q_a-Q_n^*\right)}\left\{\begin{aligned}&\frac{\left(Q_a-Q_b\right)}{\sqrt{Q_a}}\left[\tan^{-1}\left(\sqrt{\frac{Q_{n1}}{Q_a}}\right)-\tan^{-1}\left(\sqrt{\frac{Q_{n2}}{Q_a}}\right)\right]\\&+\frac{\left(Q_b-Q_n^*\right)}{\sqrt{Q_n^*}}\left[\tan^{-1}\left(\sqrt{\frac{Q_{n1}}{Q_n^*}}\right)-\tan^{-1}\left(\sqrt{\frac{Q_{n2}}{Q_n^*}}\right)\right]\end{aligned}\right\} \tag{6.25c}$$

$$C^*(V_{gs},V_{ds}) = \frac{r_{\max}}{x_t}\frac{P}{S_0^2}\left\{\frac{Q_b}{Q_a}\ln\left(\frac{Q_{n1}}{Q_{n2}}\right)+\frac{\left(Q_a-Q_b\right)}{Q_a}\ln\left(\frac{Q_a+Q_{n1}}{Q_b+Q_{n2}}\right)\right\} \tag{6.25c}$$

$$Q_a = -2\left[\frac{\varepsilon_{si}}{\beta_1}+C_{ox}\left(V_{gs}-RI_d-V_{FB}-\psi_s\right)\right], \qquad Q_b = -\frac{\beta_2 I_d}{\mu_{n0}W} \tag{6.25d}$$

$$P = -\frac{2\varepsilon_{si}}{\beta_1}\mu_{n0}W \tag{6.25e}$$

In the saturation region, the total noise power can be expressed as the sum of the noise components due to the triode region, $L\text{-}L_{sat}$, and the pinch-off region, L_{sat}. Using Equation (6.23) and integrating over each region, we can obtain

$$S_{I_d}^{sat}(f) = S_{I_d}^{linear}(f)\Big|_{V_d=V_{dsat}} + S_{I_d}^{L_{sat}}(f) \tag{6.26a}$$

with

$$S_{I_d}^{L_{sat}}(f) = \frac{qkT\cdot I_d^2}{WL^2\left(1-\dfrac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\lambda_{tun,eff}\left[2\pi\tau_{eff0}\exp\left(\lambda_{th,eff}E_{fn}\right)\right]^{(\gamma-1)}f^{\gamma}\cos\left[\dfrac{\pi}{2}(\gamma-1)\right]} \times\left[N_{TA}^{i}A_{Lsat}^{*}(V_{gs},V_{ds})+N_{TB}^{i}B_{Lsat}^{*}(V_{gs},V_{ds})+N_{TC}^{i}C_{Lsat}^{*}(V_{gs},V_{ds})\right]\cdot L_{sat} \tag{6.26b}$$

where

$$A_{Lsat}^*(V_{gs},V_{ds}) = \left(\frac{t_{ox}-x_t}{t_{ox}}\right)^2\cdot\frac{1}{\left(Q_{n,sat}+Q_n^*\right)^2} \tag{6.26c}$$

$$B^*_{Lsat}(V_{gs},V_{ds}) = \sqrt{\frac{r_{\max}}{x_t}}\left(\frac{t_{ox}-x_t}{t_{ox}}\right)\frac{1}{S_0}\cdot\frac{1}{\sqrt{Q_{n,sat}}\left(Q_{n,sat}+Q_n^*\right)} \tag{6.26d}$$

$$C^*_{Lsat}(V_{gs},V_{ds}) = \frac{r_{\max}}{x_t}\frac{1}{S_0^2}\frac{1}{Q_{n,sat}} \tag{6.26e}$$

$$Q_{n,sat} = C_{ox}\left(V_{gs} - RI_d - V_{T0} - (0.5+k_{bulk})(V_{dsat} - 2RI_d)\right) \tag{6.26d}$$

In order to incorporate a more realistic model for the trap distribution, we may use Equation (6.14) describing the conduction and valence band tails. In the linear region, it is straightforward to show that a noise contribution due to traps near the conduction band, $S^C_{I_d}(f)$, a noise contribution due to traps near the valence band, $S^V_{I_d}(f)$, and a noise contribution due to traps near the midgap, $S^M_{I_d}(f)$, are given by

$$S^C_{I_d}(f) = \frac{qkT\cdot I_d\cdot t_{ox}}{WL^2\varepsilon_{ox}\left(1-\frac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\lambda_{tun,eff}(0.5+k_{bulk})\cdot\left[2\pi\tau_{eff0}\exp(\lambda_{th,eff}E_{fn})\right]^{(\gamma-1)}\cdot f^{\gamma}\cdot\cos\left[\frac{\pi}{2}(\gamma-1)\right]}$$
$$\times\left[N^C_{TA}A^*(V_{gs},V_{ds}) + N^C_{TB}B^*(V_{gs},V_{ds}) + N^C_{TC}C^*(V_{gs},V_{ds})\right] \tag{6.27a}$$

$$S^V_{I_d}(f) = \frac{qkT\cdot I_d\cdot t_{ox}}{WL^2\varepsilon_{ox}\left(1-\frac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\lambda_{tun,eff}(0.5+k_{bulk})\cdot\left[2\pi\tau_{eff0}\exp(\lambda_{th,eff}E_{fn})\right]^{(\gamma-1)}\cdot f^{\gamma}\cdot\cos\left[\frac{\pi}{2}(\gamma-1)\right]}$$
$$\times\left[N^V_{TA}A^*(V_{gs},V_{ds}) + N^V_{TB}B^*(V_{gs},V_{ds}) + N^V_{TC}C^*(V_{gs},V_{ds})\right] \tag{6.27b}$$

$$S^M_{I_d}(f) = \frac{qkT\cdot I_d\cdot t_{ox}}{WL^2\varepsilon_{ox}\left(1-\frac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\lambda_{tun,eff}(0.5+k_{bulk})\cdot\frac{\pi}{2}\cdot f^{\gamma}}\left[N^M_{TA}A^*(V_{gs},V_{ds}) + N^M_{TB}B^*(V_{gs},V_{ds}) + N^M_{TC}C^*(V_{gs},V_{ds})\right]$$
$$\times\left\{\tan^{-1}\left[2\pi f\tau_{eff0}\exp\left(\lambda_{th,eff}E_{fn} + q\lambda_{tun,eff}t_{ox}\left(1-\frac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\right)\right] - \tan^{-1}\left[2\pi f\tau_{eff0}\exp\left(\lambda_{th,eff}E_{fn}\right)\right]\right\} \tag{6.27c}$$

with

$$N_{TA}^{C,V} = N_{T0}\left(1-\xi_{c,v}\right)\left(\frac{N_{sub}}{N_{c,v}}\right)^{\frac{T_{c,v}}{T}}, \quad N_{TB}^{C,V} = \pm N_{TA}^{C,V}\frac{2\mu_{eff}}{q}, \quad N_{TC}^{C,V} = N_{TA}\frac{\mu_{eff}^2}{q^2} \tag{6.27d}$$

$$N_{TA}^{M} = N_{T0}\frac{\left(\xi_c+\xi_v\right)}{2}, \quad N_{TB}^{M} = \pm N_{TA}^{M}\frac{2\mu_{eff}}{q}, \quad N_{TC}^{M} = N_{TA}^{M}\frac{\mu_{eff}^2}{q^2} \tag{6.27e}$$

where N_c and N_v are the effective densities of states in the conduction and valence bands, respectively.

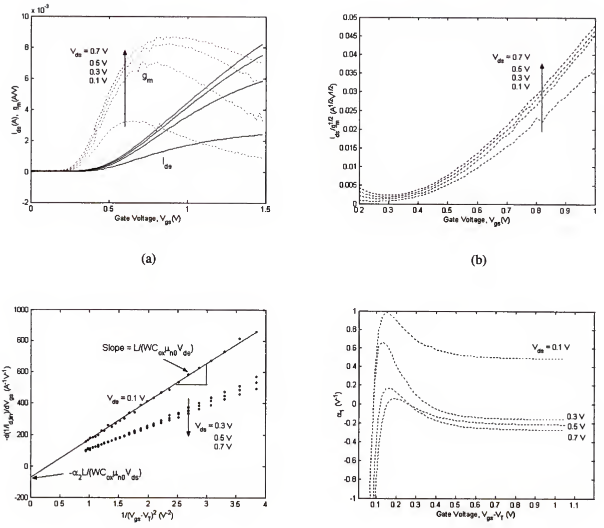
6.4 Experiments and Parameter Extraction

The devices used are n$^+$ poly-Si gate nMOSFETs which were fabricated using a remote plasma nitrided oxide (RPNO) process [Lee02, Nic00]. About 1.7–4.3 *nm* of gate oxide was grown with both furnace and rapid-thermal based processes. Nitridation was performed at room-temperature by exposing the gate oxide to a short, high-density, remote helicon-based nitrogen discharge. This was then followed by post-nitridation annealing in an inert or low partial-pressure oxygen ambient. Four terminal devices were fabricated with standard processing techniques on p-Si substrate with n$^+$ poly-Si gates, using LOCOS isolation to define the active regions.

Parameter extraction is very important for the characterization, modeling, and simulation of MOS devices and circuits. The device parameters should be extracted and determined so that the model accurately predicts experimental data. It is necessary to be careful in ultrathin oxide MOSFETs because the mobility degrades at high gate voltages resulting in a negative transconductance, as shown in Figure 6.3 (a) for the equivalent oxide thickness, $t_{ox,eq}$ = 2.2 nm. The equivalent oxide thickness $t_{ox,eq}$ can be calculated as $t_{ox,eq} = (\varepsilon_{ox}/\varepsilon_{SiON})\ t_{SiON}$, where the nitrided oxide and oxide dielectric constant, ε_{SiON} and

ε_{ox}, are assumed to be 5.7 ε_0 and 3.9 ε_0, respectively. The quadratic dependence of gate voltage through the coefficient α_2 in Equation (6.5b) accounts for the mobility degradation and the negative transconductance. Figure 6.3 (b) illustrates the typical plots of $I_{ds} / g_m^{1/2}$ as a function of the gate voltage V_{gs}. The straight line extrapolations from high gate voltages intercept the x-axis, allowing the determination of the threshold voltage V_{T0} for different drain voltages V_{ds}. It is possible to calculate the bulk charge parameter ζ in Equation (6.3) from the extracted values of $V_{T0} = 0.45$ V. In addition, obtaining ζ enables the determination of k'_{bulk} and k_{bulk} expressed in Equations (6.3) and (6.5c), respectively. It was found that ζ and k_{bulk} are 1.13 and 0.625, respectively. The low field mobility parameter μ_{n0} and the degradation parameter α_2 are extracted from Figure 6.3 (c). In high gate voltage regions, the curves show a linear relationship, allowing the determination of μ_{n0} from slope and α_2 from extrapolation to the y-axis. The extracted values of μ_{n0} and α_2 were 550 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and 0.33 V^{-2}. It is worth noting that the presence of α_2 for ultrathin oxide leads to a great impact of mobility degradation on the current-voltage and noise characteristics [Mas98]. Finally, the parasitic resistance R and the mobility degradation parameter α_0 can be obtained from plots of α_0 vs V_{gs}-V_{T0} for several values of V_{ds}. Figure 6.3 (d) is plotted substituting the extracted parameters into Equations (6.5a) – (6.5c). By plotting the constant values in high gate voltage regions as a function of V_{ds} and applying a least squares fit, $R = 6\ \Omega$ and $\alpha_0 = 0.01\ \text{V}^{-1}$ are obtained.

In ultrathin oxide MOSFETs, the two key noise parameters R_0 and S are very sensitive to the trap location and the inversion charge density. Thus, the accurate prediction of noise behavior depends on a satisfactory estimate of these parameters. Rearranging Equations (6.22a) and (6.23) for $\gamma = 1$, $E_{fn} = E_i$, and V_{gs}-$V_{T0} < 4\ \phi_b/q$, we get



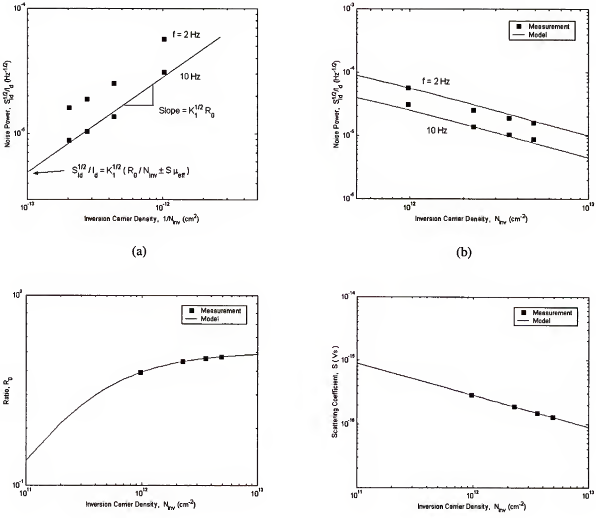
(a)

(b)

(c)

(d)

Figure 6.3 Static characteristics and parameter extraction for ultrathin oxide nMOSFET with $t_{ox,eq}$ = 2.2 nm (t_{SiON} = 3.2 nm), W = 10 μm, and L = 0.14 μm at T = 300 K. (a) transconductance g_m and drain current I_{ds} vs V_{gs} for different V_{ds}, (b) plots of $I_{ds} / g_m^{1/2}$ vs V_{gs} determining V_{T0} and ζ, (c) plots of $-d(1/I_{ds})/dV_{gs}$ vs $1/(V_{gs}-V_T)^2$ determining μ_{n0} with slope and α_2 with intercept, and (d) plots of α_1 vs V_{gs} determining R and α_0.



(a)

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Figure 6.4 Noise parameter extraction (a) plots of $S_{Id}^{1/2}$ / I_d vs $1/N_{inv}$ for the determination of R_0 with slope and S with intercept, (b) plots of $S_{Id}^{1/2}$ / I_d vs $1/N_{inv}$ for the determination of R_0 and S as a function of N_{inv} from the least squares fit, (c) plots of R_0 vs N_{inv} for extracted data and model ($x_t = 0.5\ t_{ox}$, $N_{it} = 2.0\times10^{12}$ cm^{-2}eV^{-1}) , and (d) plots of S vs N_{inv} for extracted data and model ($x_t = 0.5\ t_{ox}$, $S_0 = 8.0\times10^{9}$ cm/C$^{1/2}$Vs).

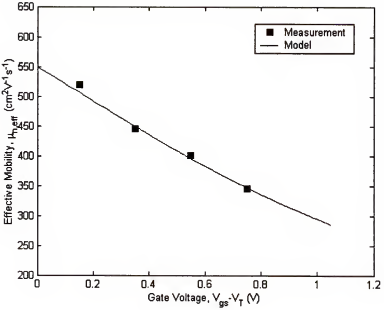
$$\frac{S_{I_d}^{1/2}(f)}{I_d} = \sqrt{\frac{kT \cdot N_{T0}}{qWL\lambda_{tun,eff} f}} \cdot \left(\frac{R_0}{N_{inv}} \pm S\mu_{eff} \right) = \sqrt{K_1} \left(\frac{R_0}{N_{inv}} \pm S\mu_{eff} \right) \tag{6.28}$$

As illustrated in Figure 6.4 (a), R_0 and S are extracted from plots of the variation of the normalized drain current $S_{Id}/I_d^{1/2}$ with $1/N_{inv}$. R_0 is determined from the slope and S is obtained by extrapolating the measured data in low density regions to the y-axis. R_0 and S were found to be 0.61 [Pac99] and 1.1×10^{-16} Vs [Van00], respectively. In order to extract R_0 and S as a function of N_{inv}, a least squares fit is applied to the measured data. The trap distance x_t and the scattering parameter S_0 determined from Figure 6.4 (b) were found to be 0.50 [Lee02] and 8.0×10^9 cm/C$^{1/2}$ Vs [Van00], respectively. Using the extracted values and the theoretical models, Equations (6.19a) and (6.21), R_0 and S are plotted as a function of N_{inv}, as shown in Figure 6.4 (c) and Figure 6.4 (d).

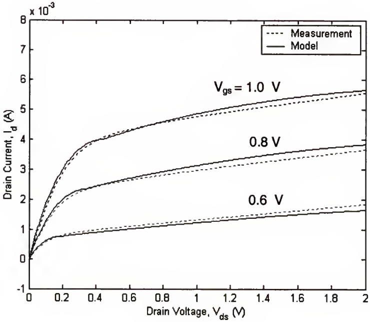
6.5 Simulation Results and Discussion

6.5.1 Static Characteristics

Prior to the noise model verification, the static characteristics are analyzed and validated by using the extracted values of mobility and *I-V* parameters. In ultrathin oxide MOSFETs, the mobility dependence on the gate voltage should be accurately modeled, since the strong normal field produces abnormal *I-V* and noise characteristics. Figure 6.5 (a) shows the comparison between the measured data and the theoretical model equation (6.5b) of effective inversion carrier mobility with respect to the gate voltage at low drain voltage. The effective mobility was calculated by using the set of parameters obtained from the extraction procedure ($V_{T0} = 0.45$ V, $k_{bulk} = 0.625$, $\mu_{n0} = 550$ cm^2 V^{-1}s^{-1}, $R = 6\ \Omega$, $\alpha_0 = 0.01$ V^{-1}, and $\alpha_2 = 0.33$ V^{-2} for nMOSFETs with $t_{ox,eq} = 2.2$ nm, $W = 10\ \mu$m, $L = 0.14\ \mu$m).



(a)



(b)

Figure 6.5 Comparison of the mobility and *I-V* models to measured data for nMOSFETs with $t_{ox,eq} = 2.2$ nm, $W = 10\ \mu m$, $L = 0.14\ \mu m$, $V_{T0} = 0.45$ V, $k_{bulk} = 0.625$, $\mu_{n0} = 550\ cm^2\ V^{-1}s^{-1}$, $R = 6\ \Omega$, $\alpha_0 = 0.01\ V^{-1}$, $\alpha_2 = 0.33\ V^{-2}$, $N_{sub} = 6\times10^{17}\ cm^{-3}$, $v_{sat} = 8\times10^6$ cm/s, and $X_j = 0.1\ \mu m$ at $T = 300$ K. (a) effective mobility $\mu_{n,eff}$ versus gate voltage V_{gs} at $V_{ds} = 50$ mV and (b) I_d-V_{ds} characteristics for V_{gs} = 0.6, 0.8, 1.0 V

It is observed that the quadratic mobility parameter α_2 enables the reproduction of the strong mobility degradation at high gate voltage. The *I-V* characteristics of both the measured data and the simulation results are plotted in Figure 6.5 (b). The simulation was carried out with the set of mobility parameters and the process parameters $N_{sub} = 6\times10^{17}$ cm^{-3} and $X_j = 0.1$ μm for $v_{sat} = 8\times10^6$ cm/s. The results clearly show an excellent agreement between the theoretical prediction of the model and the measured data in both the linear and saturation regions. This is due to the fact that the model incorporates several effects of mobility degradation, parasitic resistance, carrier velocity saturation, and channel length modulation.

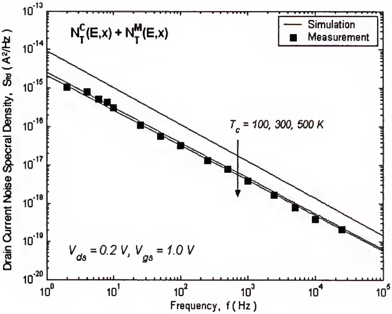
6.5.2 $1/f^{\gamma}$ Noise Characteristics

Noise measurements were performed using a HP3582A spectrum analyzer in the frequency range of 1 Hz to 25 kHz. The Brookdeal 5004 low noise voltage amplifier was used for the drain current noise. Figure 6.6 shows a typical drain current noise spectrum for nMOSFETs biased at $V_{ds} = 0.2$ V and $V_{gs} = 1.0$ V with $t_{ox,eq} = 2.2$ nm, $W = 10$ μm, and $L = 0.14$ μm. As shown in Figure 6.6 (a) and (b), the noise model was verified by the simulation results for the trap distribution $N_T^{C,M}(E,x)$ and $N_T^{i}(E,x)$ with a fitting parameter of T_c and ξ_1, respectively. It can be seen that the frequency dependence of $1/f^{\gamma}$ noise spectrum is described accurately by the trap distribution model as a function of energy and trap distance. This means that the difference in the noise behavior observed by various process technologies can be well explained by adjusting the trap-related model parameters of Equations (6.12) and (6.14).

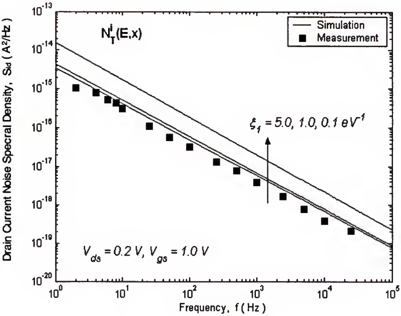
The bias dependence of the drain current noise power of the measured data and simulation results is plotted in Figure 6.7. As illustrated in Figure 6.7 (a), the noise power in the linear region shows a more gradual dependence on the gate voltage than in saturation. This behavior can be understood by different degradation of mobility with the gate voltage. Figure 6.7 (b) shows the variations of the noise power with the drain voltage for different gate voltage values. A good agreement is observed in both the linear and saturation regions.

In order to investigate the effect of the gate oxide thickness on the noise behavior in MOSFETs with direct tunneling gate leakage current, the variations of the normalized drain current noise with the oxide thickness are plotted in Figure 6.8 (a). It was confirmed that the normalized noise power decreases as the oxide thickness becomes thinner [Kol01, Mom98]. This is attributed to the fact that the noise model is based on the carrier capture-emission process via the oxide trap. In addition, the influence of the doping profile on the $1/f^{\gamma}$ noise behavior is investigated. The bulk charge parameter ζ depends on the doping profile in the near-surface region. For pMOS devices fabricated with uniformly doping, the twin-tub, and the n-well technologies, the values of ζ are 1.0, 1.4, and 1.7, respectively [Kru88]. For nMOS devices from the twin-tub and the n-well technologies, the values of ζ are 1.0 and 0.6, respectively [Kru88]. Figure 6.8 (b) shows the normalized noise power as a function of the bulk charge parameter ζ for different drain voltages in nMOSFETs. The noise power decreases with decreasing ζ, implying that a technology process with lower value of ζ is optimum for noise reduction.

The impact of the quadratic mobility parameter α_2 becomes important in thinner oxide thickness. The variations of the drain current noise power with the drain current as a parameter of α_2 are illustrated in Figure 6.9. The noise power decreases with increasing

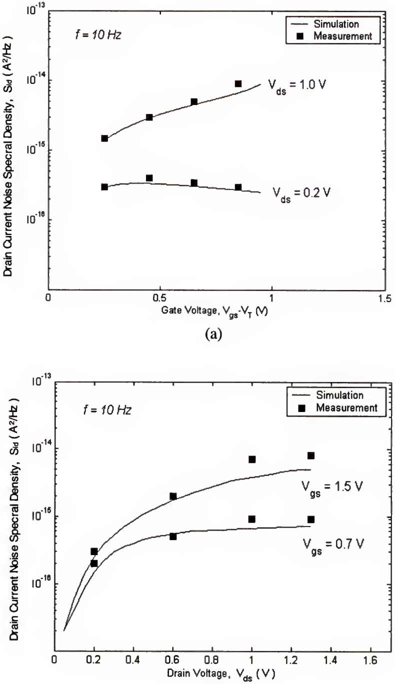


(a)



(b)

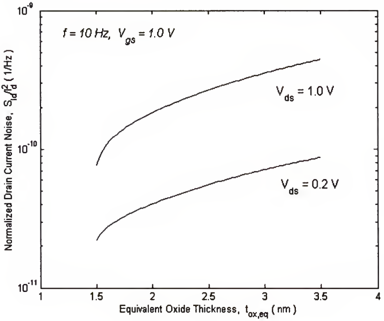
Figure 6.6 Frequency dependence of noise power S_{Id} of measured data and simulation results for (a) the trap distribution $N_T^{C,\,M}(E,x)$ with $N_{T0} = 6.25\times10^{18}$ cm^{-3}eV^{-1}, $\xi_c = \xi_v = 0.2$, $\xi_2 = 10$ V^{-1}, and $\xi_3 = -1\times10^7$ cm^{-1} and (b) the trap distribution $N_T^i(E,x)$ with $N_{T0} = 2.5\times10^{17}$ cm^{-3}eV^{-1}, $\xi_2 = 10$ V^{-1}, and $\xi_3 = -1\times10^7$ cm^{-1} for nMOSFETs with $t_{ox,eq} = 2.2$ nm, $W = 10$ μm, $L = 0.14$ μm, $V_{T0} = 0.45$ V, $k_{bulk} = 0.625$, $S_0 = 8.0\times10^9$ cm/C$^{1/2}$Vs, $\beta_1 = 8\times10^{-7}$ cm/V, and $\beta_2 = 3\times10^{-6}$ cm/V



(a)

(b)

Figure 6.7 Bias dependence of noise power S_{Id} of measured data and simulation results at f = 10 Hz as a function of (a) the gate voltage V_{gs} with the drain voltage V_{ds} as a parameter and (b) the drain voltage V_{ds} with the gate voltage V_{gs} as a parameter for nMOSFETs with $t_{ox,eq}$ = 2.2 nm, W = 10 μm, L = 0.14 μm, V_{T0} = 0.45 V, k_{bulk} = 0.625, and $S_0 = 8.0\times10^9$ cm/C$^{1/2}$ Vs. The trap distribution is assumed to be $N_T^{C,M}(E,x)$.



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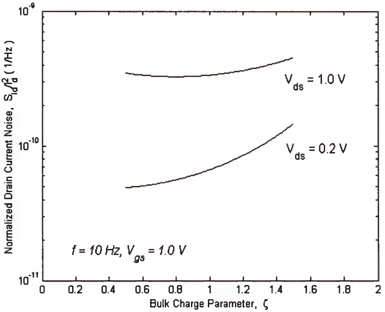


(b)

Figure 6.8 Characteristics of the normalized drain current noise. (a) Variations of the normalized drain current noise S_{Id}/I_d^2 with the equivalent oxide thickness $t_{ox,eq}$ and (b) variations of the normalized drain current noise S_{Id}/I_d^2 with the bulk charge parameter ζ in the linear and saturation. for nMOSFETs with $W = 10$ μm, $L = 0.14$ μm, $V_{T0} = 0.45$ V, $k_{bulk} = 0.625$, and $S_0 = 8.0\times10^9$ cm/C$^{1/2}$ Vs. The trap distribution is assumed to be $N_T^{C,M}(E,x)$.

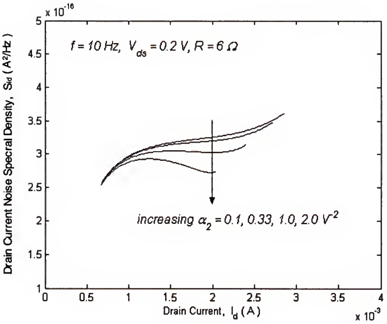


Figure 6.9 Variations of the drain current noise power S_{Id} with the drain current I_d as a parameter of the quadratic mobility degradation factor α_2 at f = 10 Hz and V_{ds} = 0.2 V.

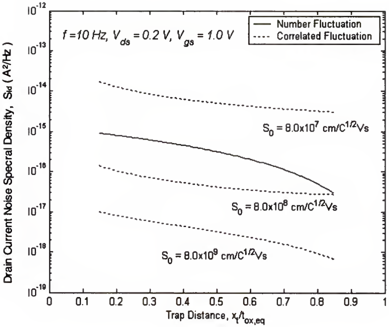


Figure 6.10 Variations of the drain current noise power S_{Id} with the normalized trap distance $x_t/t_{ox,eq}$ as a parameter of the scattering coefficient S_0 for the number fluctuation ($N_{TA}^{C,M}\ A^*$ term) and the correlated fluctuation ($N_{TB}^{C,M}\ B^* + N_{TC}^{C,M}\ C^*$ term) at V_{ds} = 0.2 V, V_{gs} = 1.0 V, and f = 10 Hz, assuming that the trap distance x_t is independent of frequency f.

α_2 at higher drain current. Therefore, the accurate extraction of α_2 is essential to the noise modeling in ultrathin oxide MOS devices [Mas98].

In order to explain a broader set of noise data, a unified 1/*f* model has been developed [Hun90a, Hun90b, Jay89, Van00]. This model is based on the fact that fluctuations in the occupancy of the oxide traps induces correlated fluctuations in the carrier number and surface mobility. As shown in Figure 6.10, the comparison of the number fluctuation, $N_{TA}{}^{C,M}\ A^*$ term in Equations (6.27), and the correlated mobility fluctuation, $N_{TB}{}^{C,M}\ B^*+N_{TC}{}^{C,M}\ C^*$ term in Equation (6.27), is demonstrated as a function of the trap distance in the linear region. The number fluctuation contribution gets smaller for the scattering coefficient $S_0 = 8.0\times10^8$ - 8.0×10^9 cm/C$^{1/2}$Vs, and gets larger for $S_0 = 8.0\times10^7$ cm/C$^{1/2}$Vs, exhibiting downward variations with the trap distance. This is mainly due to the fact that the mobility fluctuation depends on the scattering rate $S(x_t,N_{inv})$ which is larger for charge scattering sites nearer to the interface.

6.6 Conclusion

A $1/f^{\gamma}$ drain current noise model for advanced MOSFETs operating in both the linear and saturation regions was presented. Physically, the model is based on the tunneling assisted-thermally activated process of carriers, incorporating a more realistic description of trap distribution. The model includes the effects of the two-dimensional electric fields, the parasitic resistance, the doping profile, and the mobility degradation on the noise behavior. Especially, the impacts of the trap location and the inversion carrier density on both the trapping efficiency ratio and the scattering rate have been quantitatively estimated and taken into account for ultrathin oxide MOSFETs. It was shown that the noise characteristics are accurately predicted by the proposed model imposing no physical limitation on the trap distribution and trapping-detrapping process. By using the extracted model parameters, the bias dependence of the noise behavior was well described in both the linear and saturation regions. Furthermore, it was recognized from the simulation results that the effects of process technologies on the noise characteristics can be analyzed by the bulk charge parameter, the quadratic mobility degradation factor, parasitic resistance, and trap-related parameters. The results confirmed that the noise model is applicable to deep-submicron MOSFETs with ultrathin gate oxide. The model is analytically represented and therefore suitable for implementation in circuit simulators.

CHAPTER 7
CHARGE-BASED QUANTUM CORRECTION MODEL

7.1 Introduction

With the introduction of MOS devices aggressively scaled to deep submicron channel length, a ultrathin gate oxide and high doping concentration are required to increase the drive current and to minimize undesirable short channel effects. These design rules result in strong transverse electric fields at the Si-SiO_2 interface even near the threshold of inversion. This gives rise to significant band bending of the energy bands, leading to the confinement of electron motion in the direction perpendicular to the interface. In these conditions, electrons in the inversion layer form actually a quasi two-dimensional electron gas (2-DEG) with quantized energy levels within the channel [And82, Ste72]. These quantum mechanical (QM) effects have significant impact on the performance of nanoscale MOSFETs and thus the classical models are inadequate for state-of-the-art MOS structures [Bac83, Dor92, Ohk90].

The quantum nature of electrons in the inversion layer is typically studied by solving Schrödinger's and Poisson's equations self-consistently [Mog86, Ste72], and also considering the simplified models used in circuit simulators [Dor94]. A computationally efficient model, which utilizes the first three subbands in a quantized inversion layer, has been described for predicting the QM effects on the inversion layer charge density and distribution [Har92]. The enhancement in the centroid and the finite thickness of the inversion layer are one of the main QM effects on MOSFET behavior [Liu99, Lop97].

This reduces the inversion layer charge density and the total gate oxide capacitance [Lar01, Nak98, Omu00, Tak95], compared to classical models without QM effects, and causes the threshold voltage shift effect [Jan94, Ma00, Vas99].

For a compact circuit simulation model of direct tunneling of electrons form nMOS inversion layer, a variational approximation is employed to calculate the surface potential and the energy of the first quantized level in the inversion layer without the requirement for iterative solution [Cle01], and an efficient model is demonstrated by using both QM calculations for the substrate and a modified WKB approximation for the transmission probability [Yan99]. It is shown from the quantum charge sheet model that QM effects on the drain current are expected to be due to QM effects on gradients in both the inversion charge and in the surface potential [Ip98]. Based on an analytical charge-control model, the drain current model fully comprising QM effects as well as short channel effects is developed [Ma01].

Besides QM effects on the static characteristics, QM effects have been observed in the trap and noise behavior [Cel00, Luk00, Pac99, Pal97, Sie92]. For heavily doped MOSFETs, extracted interface trap capture cross sections are found to be an order of magnitude larger than values from the classical theory [Sie92]. In order to investigate QM effects on the capture and emission times of random telegraph signal (RTS) noise, the interaction between an oxide trap and an electron in the subbands of the inversion layer is theoretically modeled and analyzed in a Si-SiO$_2$ interface [Cel00, Luk00, Pal97]. Regarding the *1/f* noise models of drain current, numerical models are employed to account for QM impact on the extracted value of the oxide trap density [Pac99].

However, there are no analytical 1/*f* and thermal noise models, which incorporate QM effects and are applicable to circuit simulations.

In this Chapter, we will present a charge-based quantum correction model for current and noise in nanoscale MOSFETs. Section 7.2 describes the quantization effects on the inversion charge parameters, such as the surface potential, the threshold voltage, the inversion charge density, and gate capacitance model. In Section 7.3, on the basis of the quantum correction model of the inversion layer charge, a gate leakage current and 1/*f* noise model are formulated. Section 7.4 gives the analytical expressions for the drain current and noise model accounting for quantum and short channel effects. The quantized charge parameters are calculated from the lowest energy level, and the comparison between the classical and quantum models is shown in Section 7.5. Finally, Section 7.6 presents some conclusions.

7.2 Quantum Correction for Compact Modeling

7.2.1 Schrödinger-Poisson's Equations

The high channel doping levels and large transverse electric fields result in the confinement of electron motion in the *x* direction perpendicular to the interface, so that the conduction band within the channel is split into discrete subbands. Based on the effective mass approximation and a parabolic band structure, the envelope wave function ζ_{ij} for the *i*th valley and *j*th subband satisfies 1-D Schrödinger's equation [Ans82, Ste72]

$$\left[-\frac{\hbar^2}{2m_{xi}}\frac{d^2}{dx^2}+q\psi(x)\right]\zeta_{ij}(x)=E_{ij}\zeta_{ij}(x) \tag{7.1}$$

where q is the electron charge, $\hbar$ is the reduced Planck constant, m_{xi} is the effective mass perpendicular to the surface ($m_{x1} = 0.916\ m_0$, $m_{x2} = 0.19\ m_0$), E_{ij} is the energy state of the ith valley and jth subband, and $\psi(x)$ is the electrostatic potential which is the solution of 1-D Poisson's equation

$$\frac{d^2\psi(x)}{dx^2} = -\frac{q}{\varepsilon_{si}}\left[p(x) - n(x) + N_d^+(x) - N_a^-(x)\right] \tag{7.2}$$

where ε_{si} is the silicon dielectric constant, $n(x)$ is the electron density, $p(x)$ is the hole density, and $N_d^+(x)$ and $N_a^-(x)$ are the donor and acceptor concentrations, respectively. By solving Equations (7.1) and (7.2) self-consistently under appropriate boundary conditions, the 2-D electron density of the inversion layer is obtained by summing over all subbands as follows [Har92, Ste72]

$$n(x) = \sum_{i,j} N_{ij}\left|\zeta_{ij}(x)\right|^2 = \frac{kT}{\pi\hbar^2}\sum_{i,j} g_i m_{di} \ln\left[1 + \exp\left(\frac{E_f - E_{ij}}{kT}\right)\right]\left|\zeta_{ij}(x)\right|^2 \tag{7.3}$$

with

$$E_f - E_{ij} = q\psi_s - \frac{E_g}{2} - q\phi_f - E_{ij} \tag{7.4a}$$

$$E_{ij} = \left(\frac{\hbar^2}{2m_{xi}}\right)^{1/3}\left[\frac{3}{2}q\pi F_s(\psi_s)\cdot\left(j + \frac{3}{4}\right)\right]^{2/3} \quad for\ \ j = 0,1,2,\cdots \tag{7.4b}$$

$$F_s(\psi_s) = \sqrt{\frac{2qN_{sub}}{\varepsilon_{si}}}\left[\left(v_{th}\exp\left(-\frac{\psi_s}{v_{th}}\right) + \psi_s - v_{th}\right) + \exp\left(-\frac{2\phi_f}{v_{th}}\right)\cdot\left(v_{th}\exp\left(\frac{\psi_s}{v_{th}}\right) - \psi_s - v_{th}\right)\right]^{1/2} \tag{7.4c}$$

where k is the Boltzmann's constant, T is the temperature, g_i is the degeneracy of the energy subband ($g_1 = 2$, $g_2 = 4$), m_{di} is the density-of-states effective mass ($m_{d1} = m_{x2}$,

$m_{d2} = (m_{x1}m_{x2})^{1/2}$), E_f is the Fermi energy level, $\phi_f = v_{th}\ln(N_{sub}/n_i)$ is the Fermi potential, ψ_s is the surface potential, E_g is the energy bandgap, F_s is the surface electric field, $v_{th} = kT/q$ is the thermal voltage, N_{sub} is the substrate doping density, n_i is the intrinsic carrier density, and N_{ij} is the sheet charge density for the jth subband from the ith valley.

7.2.2 Surface Potential and Threshold Voltage Model

Due to the nonzero value of the quantized charge centroid, the surface potential determined by quantum effects is greater than predicted by the classical model [Dor94]. Multiplying the Poisson equation (7.2) by x and integrating it, we get

$$\psi_s = \frac{q}{\varepsilon_{si}}\int_0^{x_{dep}} x \cdot N_a^-(x)dx + \frac{qN_n^{QM}(\psi_s)\cdot x_n^{QM}(\psi_s)}{\varepsilon_{si}} \tag{7.5}$$

with

$$N_n^{QM}(\psi_s) = \sum_{ij} N_{ij}(\psi_s) \tag{7.6a}$$

$$x_n^{QM}(\psi_s) = \frac{\sum_{ij} N_{ij}x_{ij}}{N_n^{QM}(\psi_s)}, \qquad x_{ij} = \frac{2E_{ij}}{3qF_s(\psi_s)} \tag{7.6b}$$

where x_{dep} is the depletion layer width, Q_n is the total electron charge density, and x_n^{QM} is the average centroid position from the interface. Therefore, it is observed from Equation (7.5) that the enhancement of the surface potential is given by [Lop97]

$$\Delta\psi_s^{QM} = \frac{Q_n^{QM}(\psi_s)\cdot x_n^{QM}(\psi_s)}{\varepsilon_{si}} \tag{7.7}$$

Due to the quantum-mechanical behavior of inversion layer electrons, more band bending is required to achieve the same inversion charge as the classical value, resulting in the increase in the threshold voltage. The threshold voltage V_T can be easily calculated by including an additional quantum shift term as follows [Ma00, Ma01]

$$V_T^{QM} = V_T + \Delta V_T^{QM} \tag{7.8}$$

with

$$\Delta V_T^{QM} = \Delta \psi_s^{QM}\Big|_{\psi_s=2\phi_f} \cdot \left(1 + \frac{1}{2C_{ox}}\sqrt{\frac{\varepsilon_{si} q N_{sub}}{\phi_f}}\right) \tag{7.9}$$

For the polysilicon-SiO$_2$-p-Si MOS structure, the relationship between the gate-to-source voltage V_{gs} and the surface potential ψ_s is classically described by [Cle01, Lar01, Mas02]

$$V_{gs} = V_{FB} + \psi_s + V_{poly} + \frac{Q_s(\psi_s)}{C_{ox}} + \frac{Q_{it}}{C_{ox}} \tag{7.10}$$

with

$$V_{poly} = \frac{1}{2m}\left[\sqrt{1 + 4m(V_{gs} - V_{fb} - \psi_s)} - 1\right] \quad m = \frac{\varepsilon_{ox}^2}{2q\varepsilon_{si} N_{poly} t_{ox}^2} \tag{7.11}$$

where V_{FB} is the flat-band voltage, V_{poly} is the polysilicon voltage drop, N_{poly} is the polysilicon doping concentration, C_{ox} is the oxide capacitance per unit area, ε_{ox} is the oxide dielectric constant, t_{ox} is the oxide thickness, Q_s is the total charge in the semiconductor per unit area, and the trapped charge in the oxide, Q_{it}, is included to account for the trapping-detrapping effects at the Si-SiO$_2$ interface. In order to obtain the quantum model, it is necessary to replace the classical Q_s with the quantized charge density as follows

$$V_{gs} = V_{FB} + \psi_s^{QM} + V_{poly} + \frac{qN_n^{QM}(\psi_s^{QM}) + Q_d(\psi_s^{QM})}{C_{ox}} + \frac{Q_{it}}{C_{ox}} \tag{7.12}$$

where Q_d is the depletion charge density per unit area.

7.2.3 Inversion Charge and Capacitance Model

As the channel length and oxide thickness continue to be scaled to nanometer range in current CMOS devices, the quantization effects should be taken into account for an accurate inversion charge model. By using Equations (7.5), (7.7), and (7.12), an expression for the inversion layer charge is obtained as

$$Q_{n0}^{QM}(\psi_s^{QM}) = C_{ox}^{QM}\left(V_{gs} - V_{FB} - \psi_s^{QM} - \Delta\psi_s^{QM} - V_{poly} - \frac{Q_d + Q_{it}}{C_{ox}}\right) = C_{ox}^{QM}\left(V_{gs} - V_T^{QM}\right) \tag{7.13}$$

with

$$C_{ox}^{QM} = \frac{\varepsilon_{ox}}{t_{ox}^{QM}} = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} x_n^{QM}} \tag{7.14}$$

where the denominator t_{ox}^{QM} of Equation (7.14) is termed the electrical oxide thickness. Including the parasitic source and drain resistance $R_{s,d}$ and incorporating the drain-to-source voltage V_{ds}, the channel charge density is expressed by

$$Q_n^{QM}(y) = C_{ox}^{QM} \cdot \left(V_{gs} - I_d R_{s,d} - V_T^{QM} - 2k_{bulk} V_y(y)\right) \tag{7.15}$$

where I_d is the drain current, $V_y(y)$ is the channel potential at any given point y along the channel and k_{bulk} is the bulk charge parameter.

Since the quantum effects lead to an increase in the inversion layer thickness, the inversion capacitance decreases and thus, the total gate capacitance is reduced. The inversion charge capacitance is given by [Liu99, Ma01]

$$\frac{1}{C_n^{QM}}=\frac{1}{C_n}+\frac{X^{QM}}{\varepsilon_{si}} \tag{7.16}$$

with

$$X^{QM}=\frac{\int x\cdot n(x)dx}{\int n(x)dx}=\frac{5.047+0.771E_{eff}}{0.113+E_{eff}} \tag{7.17a}$$

$$E_{eff}=\frac{1}{2t_{ox}}\left[n_{sw}v_{th}\ln\left(1+\exp\left(\frac{V_{gs}-V_{poly}-V_T}{n_{sw}v_{th}}\right)\right)+2\left(V_T-V_{FB}-2\phi_f\right)\right] \tag{7.17b}$$

$$n_{sw}=1+\sqrt{\frac{\varepsilon_{si}qN_{sub}}{4\phi_f C_{ox}^2}} \tag{7.17c}$$

where C_n is the classical inversion capacitance, X^{QM} is the inversion layer thickness, E_{eff} is the effective electric field in inversion layer in MV/cm, and n_{sw} is the subthreshold swing parameter. For very high polysilicon doping levels ($N_{poly} > 1\times10^{19}$ cm^{-3}), no quantum behavior has to be considered to determine the surface potential at the polysilicon-SiO$_2$ interface, because the all the subbands are squeezed out of the potential well [Lar01]. According to the classical theory, the polysilicon capacitance is calculated by differentiating the polysilicon charge density Q_{poly} as follows [Lar01]

$$C_{poly}=\frac{\sqrt{2\varepsilon_{si}qN_{poly}}\left[\exp\left(\frac{V_{poly}}{v_{th}}\right)-1\right]}{\sqrt{v_{th}\exp\left(\frac{V_{poly}}{v_{th}}\right)+V_{poly}-v_{th}}} \tag{7.18}$$

7.3 Quantum Effects on Gate Leakage Current and Noise Model

7.3.1 Gate Leakage Current Model

In the ultrathin gate oxide regime (< 3nm), the classical models without including quantum effects of the inversion layer overestimate the value of the gate leakage current and noise, because the peak charge density is situated at a distance (≈ 1 nm) away from the Si-SiO$_2$ interface. This leads to an enhancement in the oxide thickness and a reduction in the oxide voltage. Therefore, the quantum effects need to be taken into account by using the correction for the oxide thickness and the oxide voltage,

$$V_{ox}^{QM} = V_{gs} - V_{FB} - \psi_s^{QM} - V_{poly} - \frac{Q_{it}}{C_{ox}} \tag{7.19}$$

The BSIM4 gate tunneling current model can predict all the significant direct tunneling current components which are electron tunneling from the conduction band in the substrate to the gate, electron tunneling from the valence band in the substrate to the gate, and hole tunneling from the valence band in the gate to the substrate. Taking into account quantum effects of the oxide thickness and the oxide voltage, the BSIM4 tunneling current model becomes [Lee02]

$$J_{DT,BSIM}^{QM} = \frac{q^3}{8\pi h \phi_b \varepsilon_{ox}} \cdot C^{QM}(t_{ox}^{QM}, V_{ox}^{QM}) \cdot \exp\left[-\frac{8\pi\sqrt{2m_{ox}}\phi_b^{3/2} t_{ox}^{QM} [1-(1-\left|V_{ox}^{QM}\right|/\phi_b)^{3/2}]}{3hq\left|V_{ox}^{QM}\right|} \right] \tag{7.20}$$

with

$$C^{Qm}(t_{ox}^{QM}, V_{ox}^{QM}) = \exp\left[\frac{20}{\phi_b} \left(\frac{\left|V_{ox}^{QM}\right| - \phi_b}{\phi_{bo}} + 1 \right)^{\lambda} \cdot \left(1 - \frac{\left|V_{ox}^{QM}\right|}{\phi_b} \right) \right] \cdot \left(\frac{V_{gs}}{t_{ox}^{QM}} \right) \cdot N^{QM} \tag{7.21a}$$

$$N^{QM} = \frac{\varepsilon_{ox}}{t_{ox}^{QM}} \left\{ n_{sw} \ln\left[1+\exp\left(\frac{V_{gs}-V_{poly}}{n_{sw}}\right)\right] + v_{th} \ln\left[1+\exp\left(-\frac{V_{gs}-V_{fb}}{v_{th}}\right)\right]\right\} \qquad (7.21b)$$

where h is the Planck constant, m_{ox} is the electron effective mass of the conduction band in the oxide, λ is a fitting parameter for three current components, ϕ_{bo} is the Si-SiO$_2$ barrier height (3.1 eV for electrons and 4.5 eV for holes), and ϕ_b is the tunneling barrier height.

7.3.2 Gate Current Noise Model

One possible mechanism for $1/f^{\gamma}$ noise of the gate leakage current is for traps to affect locally the barrier height or shape due to thermal noise of the frequency-dependent conductance of the oxide slow traps [Lee03]. This fluctuation in turn modulates the tunneling transmission, and causes fluctuations in the tunneling current. The quantum effects for the spectral noise density are accounted for by the correction of the oxide voltage V_{ox} and the electron subband energy E_{ij}, and are described by [Lee03]

$$\left.\frac{S_{I_g}^{1/f}(f)}{I_g^2}\right|^{QM} = \frac{\dfrac{G_p^{QM}(f)}{2\pi f}}{\left[\dfrac{G_p^{QM}(f)}{2\pi f}\right]^2 + \left[C_{ox}^{QM} + C_p^{QM}(f)\right]^2} \cdot \frac{1}{f} \cdot A^{QM}(V_{ox}^{QM}) \cdot \sum_{ij} B_{ij}^{QM}(V_{ox}^{QM}, E_{ij}) \qquad (7.22)$$

with

$$A^{QM}(V_{ox}^{QM}) = \frac{16 m_{ox} kTq^2}{9\pi\hbar^2 A_g (t_{ox}^{QM})^2 (X_2^{QM})^4} \qquad (7.23a)$$

$$\begin{aligned} B_{ij}^{QM}(V_{ox}^{QM}, E_{ij}) = {} & \sqrt{X_{1,ij}^{QM}(X_{1,ij}^{QM} - qV_{ox}^{QM})}\left[8X_{1,ij}^{QM}(X_{1,ij}^{QM} - qV_{ox}^{QM}) - 3q^2(V_{ox}^{QM})^2\right] \\ & - 2\left[2(X_{1,ij}^{QM})^2(2X_{1,ij}^{QM} - 3qV_{ox}^{QM}) + q^3(V_{ox}^{QM})^3\right] \end{aligned} \qquad (7.23b)$$

$$X_{1,ij}^{QM} = \phi_b + E_{fs} - E_{ij} + \frac{m_\perp}{m_{ox}} E_\perp, \quad X_2^{QM} = q\frac{V_{ox}^{QM}}{t_{ox}^{QM}} \tag{7.23c}$$

where $m_\perp$ is the transversal electron effective mass, $E_\perp$ is the transversal energy component, A_g is the gate tunneling area, $G_p^{QM}(f)$ and $C_p^{QM}(f)$ are the frequency-dependent parallel conductance and capacitance of oxide traps, respectively. Assuming that the oxide trap density is spatially distributed over a physical distance d into the oxide, the electrical trap distance d^{QM} becomes $d+(\varepsilon_{ox}/\varepsilon_{si})x_n^{QM}$ in the quantum approach, leading to

$$\frac{G_p^{QM}(f)}{2\pi f} = \left.\frac{G_p(f)}{2\pi f}\right|_{d\to d^{QM}}, \quad C_p^{QM}(f) = \left.C_p(f)\right|_{d\to d^{QM}} \tag{7.24}$$

7.4 Quantum Effects on Drain Current and Noise Model

7.4.1 Mobility and Drain Current Model

As the gate oxide thickness and the substrate doping level are thinner and higher, the normal electric field increases significantly and the influence of the quantized inversion layer become important. A correct and simple model to account for these effects is required to predict the mobility and *I-V* characteristics of nanoscale MOSFETs. The quadratic mobility degradation factor is necessary for an effective mobility model of ultrathin gate oxide nMOSFETs, and an analytical mobility model $\mu_{n,eff}^{QM}$ is given by [Mas98]

$$\mu_{n,eff}^{QM} = \frac{\mu_{n0}}{1+\alpha_1^{QM}\left(\dfrac{V_{gs}-V_T^{QM}-k_{bulk}V_{ds}}{t_{ox}^{QM}}\right)+\alpha_2^{QM}\left(\dfrac{V_{gs}-V_T^{QM}-k_{bulk}V_{ds}}{t_{ox}^{QM}}\right)^2} \tag{7.25}$$

where μ_{n0} is the low-field electron mobility, and α_1^{QM} and α_2^{QM} are the mobility degradation factor. Introducing an effective drain-to-source voltage $V_{ds,eff}^{QM}$, and considering the channel length shortening effects and parasitic resistance $R_{s,d}$, the drain current for short-channel MOSFETs biased in the linear and saturation region is then obtained as [Cho92, Ma01]

$$I_{d,total}^{QM} = \frac{W}{L}\mu_{n,eff}^{QM}C_{ox}^{QM}\frac{\left(V_{gs} - V_T^{QM} - k_{bulk}V_{ds,eff}^{QM}\right)\cdot V_{ds,eff}^{QM}}{\left(1+\frac{V_{ds,eff}^{QM}}{E_c L}\right)+\frac{W}{L}\mu_{n,eff}^{QM}C_{ox}^{QM}R_{s,d}V_{ds,eff}^{QM} - \frac{L_{sat}}{L}} \tag{7.26}$$

with

$$V_{ds,eff}^{QM} = \frac{1}{2}\left(V_{ds} + (1+\Delta)V_{dsat}^{QM}\right) - \sqrt{\frac{1}{4}\left(V_{ds} + (1+\Delta)V_{dsat}^{QM}\right)^2 - V_{ds}\cdot V_{dsat}^{QM}} \tag{7.27a}$$

$$V_{dsat}^{QM} = V_{dsat}\Big|_{C_{ox}\to C_{ox}^{QM},\,V_T\to V_T^{QM}} \tag{7.27b}$$

where W is the channel width, L is the channel length, E_c is the lateral critical electric field at which carriers travel with the saturated velocity v_{sat} near the drain section of the length L_{sat}, and Δ is a small quantity to adjust the smoothness at the transition region near V_{dsat} [Cho92].

7.4.2 RTS (Random Telegraph Signal) Noise Model

If we consider a section of channel with width W and length Δy, fluctuations in the trapped oxide charge will induce correlated fluctuations in the channel carrier number and mobility. The resulting fractional change in the local drain current can be represented as [Hun90b]

$$\frac{\Delta I_d}{I_d} = -\left(\frac{1}{\Delta Q_n} \cdot \frac{\delta \Delta Q_n}{\delta \Delta Q_T} \pm \frac{1}{\mu_{n,eff}} \cdot \frac{\delta \mu_{n,eff}}{\delta \Delta Q_T} \right) \cdot \delta \Delta Q_T \tag{7.28}$$

where $\Delta Q_n = Q_n W \Delta y$, $\Delta Q_T = Q_T W \Delta y$, and Q_n and Q_T are total charge of channel carriers and occupied traps per unit area. The sign of the mobility term is chosen either positive for acceptor-like traps or negative for donor-like traps. The ratio $R_0 = -\delta \Delta Q_n / \delta \Delta Q_T$ in Equation (7.28) describes the efficiency of the drain current modulation corresponding to a variation of the trapped charge. Considering the effects of the quantization and polysilicon depletion, the coefficient R_0^{QM} depends on the surface potential through charge capacitance and is given by [Hun90b]

$$R_0^{QM} = \frac{C_n^{QM}}{C_{ox}^{QM} + C_n^{QM} + C_d^{QM} + C_{poly} + C_{it}} = \frac{Q_n^{QM}}{Q_n^{QM} + Q_n^{QM*}} \tag{7.29}$$

with

$$C_n^{QM} \approx \frac{q}{kT} Q_n^{QM}, \qquad Q_n^{QM*} = \frac{kT}{q}\left(C_{ox}^{QM} + C_d^{QM} + C_{poly} + C_{it} \right) \tag{7.30}$$

where C_{it} is the interface trap capacitance. On the basis of Matthiessen's rule [Jay89], we can readily find that

$$\delta \mu_{n,eff} = \mu_{n,eff}^2 S^{QM}\left(x_t^{QM}, Q_n^{QM} \right) \cdot \frac{\delta \Delta Q_T}{q W \Delta y} \tag{7.31}$$

where $S^{QM}\left(x_t^{QM}, Q_n^{QM} \right)$ is a scattering rate which is a function of the distance $x_t^{QM} \left(= x_t + (\varepsilon_{ox} / \varepsilon_{si}) x_n^{QM} \right)$ of the trapping state [Jay89] and of the carrier charge density Q_n^{QM} [Van00], and is strongly affected by channel quantization [Pac99]. In order to properly account for these effects in ultrathin oxide MOSFETs, we employ an empirical model for the scattering coefficient $S^{QM}\left(x_t^{QM}, Q_n^{QM}\right)$ in linear approximation as [Jay89, Van00]

$$S^{QM}(x_t^{QM}, Q_n^{QM}) = S_1 - S_2 \ln\left(\frac{Q_n^{QM}}{q}\right) + S_3 \ln\left(\frac{r_{\max}}{x_t^{QM}}\right) \approx \frac{1}{S_0 \sqrt{x_t^{QM} / r_{\max}^{QM}} \cdot \sqrt{Q_n^{QM}}} \tag{7.32}$$

where $r_{\max}^{QM} \approx (\varepsilon_{ox} + \varepsilon_{si}) / \left(C_{ox}^{QM} + C_d^{QM} + C_{it}\right)$ is the maximum distance from the scattering charge for which the effect of image charges* can be neglected and S_0 is the scattering constant in cm/C$^{1/2}$Vs. Assuming that the carrier distribution is uniform along the channel, the RTS amplitude noise becomes [Cel00]

$$\frac{\Delta I_d}{I_d} = -\frac{1}{WL}\left(q \frac{R_0^{QM}}{Q_n^{QM}} \cdot \pm S^{QM}\left(x_t^{QM}, Q_n^{QM}\right) \cdot \mu_{n,eff}^{QM}\right) \tag{7.33}$$

7.4.3 Low and High Frequency Noise Model

According to the number fluctuation theory, the total power spectral density of the drain current noise at low frequencies is obtained by calculating the fluctuations in the number of occupied traps and performing the integration over the channel length. Assuming that the oxide trap density $N_t(E)$ is uniformly distributed over the space into the oxide and the trapping time constant is an exponentially increasing function of the trap distance x_t, the total $1/f$ noise power of the drain current in the linear region ($V_d \leq V_{dsat}$) is given by [Hun90b]

$$S_{I_d}^{1/f}(f)\Big|_{Lin}^{QM} = \frac{kTq^2 I_d^{QM} \mu_{n,eff}^{QM}}{2k_{bulk}\gamma_{tun} f L^2 C_{ox}^{QM}}\left[A^{QM} \ln\left(\frac{Q_{n0}^{QM} + Q_n^{QM*}}{Q_{nL}^{QM} + Q_n^{QM*}}\right) + \frac{B^{QM}}{q}\left(Q_{n0}^{QM} - Q_{nL}^{QM}\right) + \frac{C^{QM}}{2q^2}\left((Q_{n0}^{QM})^2 - (Q_{nL}^{Qm})^2\right)\right] \tag{7.34}$$

with

$$A^{QM} = N_t(E_{fn}),\ \ B^{QM} = \frac{2S^{QM}\mu_{n,eff}^{QM}}{R_0^{QM}} N_t(E_{fn}),\ \ C^{QM} = \left(\frac{S^{QM}\mu_{n,eff}^{QM}}{R_0^{QM}}\right)^2 N_t(E_{fn}) \tag{7.35a}$$

$$Q_{n0}^{QM} = C_{ox}^{QM}\left(V_{gs} - V_T^{QM}\right),\quad Q_{nL}^{QM} = C_{ox}^{QM}\left(V_{gs} - V_T^{QM} - 2k_{bulk}V_{ds}\right) \tag{7.35b}$$

where $\gamma_{tun} \approx 10^8$ cm^{-1} is the exponential factor of tunneling process, $N_t(E_{fn})$ is the oxide trap density around the electron quasi-Fermi level E_{fn}, and Q_{n0}^{QM} and Q_{nL}^{QM} are carrier charge densities for $R_{s,d} = 0$ at the source and drain ends of the channel, respectively. In the saturation region, the total *1/f* noise power is obtained by including the noise contribution arising from the pinch-off region L_{sat}, and is represented as [Hun90b]

$$S_{I_d}^{1/f}(f)\Big|_{Sat}^{QM} = S_{I_d}^{1/f}(f)\Big|_{Lin}^{QM} + L_{sat}\frac{kT\left(I_d^{QM}\right)^2}{\gamma_{tun} fWL^2}\frac{q^2A^{QM} + qB^{QM}Q_{nL}^{QM} + C^{QM}\left(Q_{nL}^{QM}\right)^2}{\left(Q_{nL}^{QM} + Q_n^{QM*}\right)^2} \tag{7.36}$$

with

$$Q_{n0}^{QM} = C_{ox}^{QM}\left(V_{gs} - V_T^{QM}\right),\quad Q_{nL}^{QM} = C_{ox}^{QM}\left(V_{gs} - V_T^{QM} - 2k_{bulk}V_{dsat}\right) \tag{7.37}$$

It has been shown that the high frequency noise originates from thermal fluctuation in the channel and is expresses as [Wan94]

$$S_{I_d}^{Thermal} = 4kT \cdot \frac{\mu}{L^2} \cdot Q_n\left(V_{gs}, V_{ds}\right) \tag{7.38}$$

where Q_n is the total inversion layer charge density. For the thermal noise modeling of short channel devices, the total inversion charge density is derived by considering the velocity saturation of carriers due to the high lateral electric field, and is turned out to be [Wan94]

$$Q_n^{QM}\left(V_{gs},V_{ds}\right)=\frac{W^2\mu_{eff}^{QM}\left(C_{ox}^{QM}\right)^2}{I_d^{QM}}\left[\left(V_{gs}-V_T^{QM}\right)^2V_{ds}-2k_{bulk}\left(V_{gs}-V_T^{QM}\right)V_{ds}^2+\frac{4}{3}k_{bulk}^2V_{ds}^3\right]$$
$$-\frac{WC_{ox}^{QM}}{E_c}\left[\left(V_{gs}-V_T^{QM}\right)V_{ds}-k_{bulk}V_{ds}^2\right] \tag{7.39}$$

Substituting Equation (7.39) into Equation (7.38), the thermal noise spectral densities of drain current in the linear and saturation region are given by

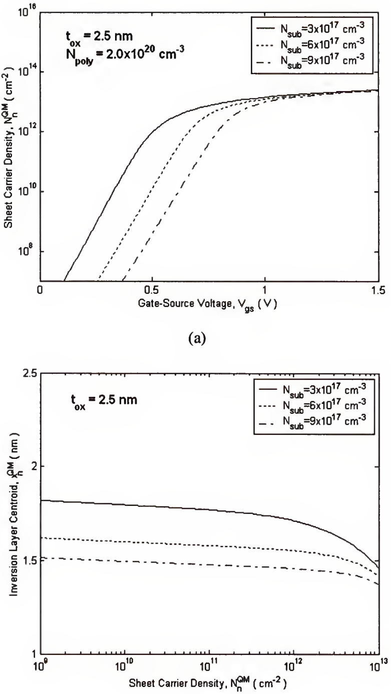
$$S_{I_d}^{Thermal}\Big|_{Lin}^{QM}=4kT\cdot\frac{\mu_{n,eff}^{QM}}{L^2}\cdot Q_n^{QM}\left(V_{gs},V_{ds}\right) \tag{7.40a}$$

$$S_{I_d}^{Thermal}\Big|_{Sat}^{QM}=4kT\cdot\frac{\mu_{n,eff}^{QM}}{(L-L_{sat})^2}\cdot Q_n^{QM}\left(V_{gs},V_{dsat}\right) \tag{7.40b}$$

7.5 Results and Discussion

For the purpose of developing a model applicable to circuit simulation, it is very important to extend classical simulators to include QM effects with computational efficiency. For the quantized energy levels of inversion layers, a simple and approximate model can be obtained by considering the dominant contribution of carriers in the lowest energy subbands E_{10} [Cle01, Dor94]. Figure 7.1 shows the quantized charge parameters calculated from the lowest energy level E_{10} for the substrate doping concentrations, N_{sub} = 3×10^{17} cm^{-3}, 6×10^{17} cm^{-3}, and 9×10^{17} cm^{-3}. As the gate-source voltage increases, the sheet carrier density N_n^{QM} in the energy level E_{10} increases and the inversion layer centroid x_n^{QM} moves more closely to the Si-SiO$_2$ interface for each doping concentrations, as shown in Figure 7.1 (a) and (b), respectively. These results are confirmed by numerical results and other models [Cle01, Lop97, Ohk90]. The QM effects on the surface potential and the threshold voltage are depicted in Figure 7.2. Figure 7.2 (a) clearly illustrates that, at higher gate-source voltage and thinner oxide thickness, the transverse electric field increases appreciably and thus the energy gap between the bottom of the conduction band and the lowest energy level is enhanced, leading to noticeable QM effects [Cle01, Dor94, Ma01]. It is obvious from Equation (7.9) that the threshold voltage shift due to QM effects becomes more pronounced as the oxide thickness and the substrate doping concentration increase, as shown in Figure 7.2 (b). Figure 7.3 (a) and (b) show the inversion charge density and capacitance as a function of the gate-source voltage according to the classical and QM models, respectively. The deviation between the classical and QM models for the inversion charge density increases significantly for higher doping concentration, and for the inversion layer capacitance, the results coincide in weak inversion and deviate in strong inversion [Bac83].

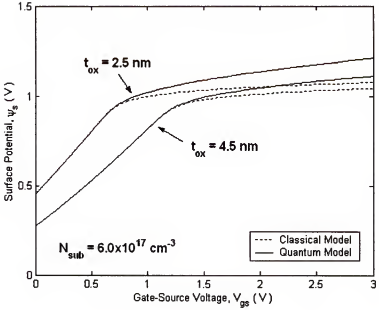
By considering the QM effects on the oxide voltage and the oxide thickness, the gate leakage tunneling current and noise model can be formulated. The oxide voltage due to QM effects is calculated using the additional surface potential to achieve the same inversion charge as the classical value, as shown in Figure 7.4 (a). For ultrathin oxide MOS structure, the oxide thickness shift due to QM effects has a greater impact on the gate tunneling current than the oxide voltage shift due to QM effects. Therefore, the extraction procedure of the electrical oxide thickness accounting for QM effects is required to accurately predict the tunneling current through the gate oxide. The use of the physical oxide thickness ignoring QM effects leads to erroneous results in the calculation of the gate tunneling current, as shown in Figure 7.4 (b). Quantitatively, it is found from Equation (7.22) that the exact knowledge of the oxide thickness is also essential to the evaluation of the gate current noise model. As illustrated in Figure 7.5 (a), the deviation



(a)

(b)

Figure 7.1 Quantized charge parameters calculated from the lowest energy level E_{10} for three substrate doping concentrations. (a) sheet carrier density N_n^{QM} as a function of the gate-source voltage V_{gs} and (b) inversion layer centroid position from the Si-SiO$_2$ interface, x_n^{QM}, as a function of N_n^{QM} (V_{FB} = -0.9 V, T = 300 K)



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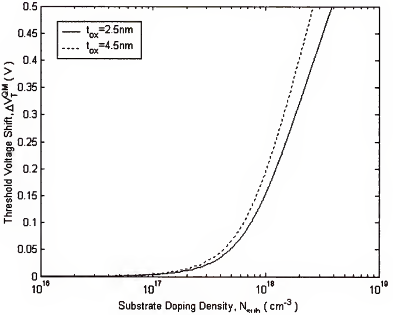
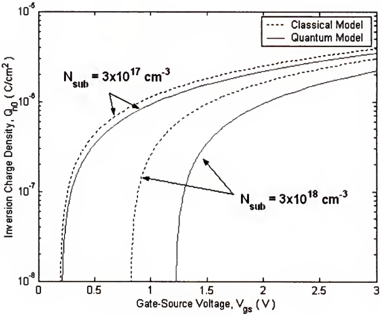


(b)

Figure 7.2 Quantum effects on (a) the surface potential ψ_s versus the gate-source voltage V_{gs} and (b) the additional threshold voltage shift ΔV_T^{QM} versus the substrate doping density N_{sub} for t_{ox} = 2.5 and 4.5 nm. (V_{FB} = -0.9 V, $E_{ij} = E_{10}$, $N_{it} = 2\times10^{11}$ cm^{-2}, $N_{poly} = 2\times10^{20}$ cm^{-3}, T = 300 K)



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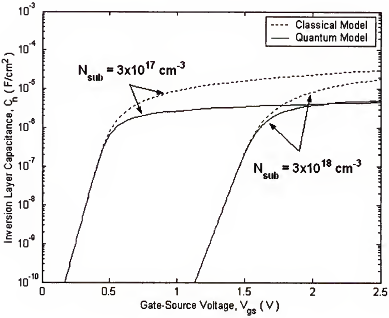
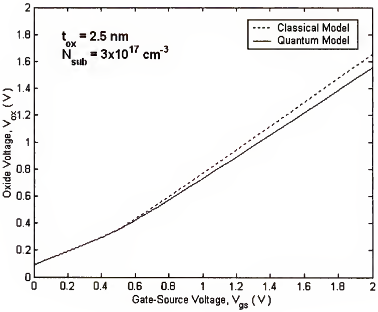
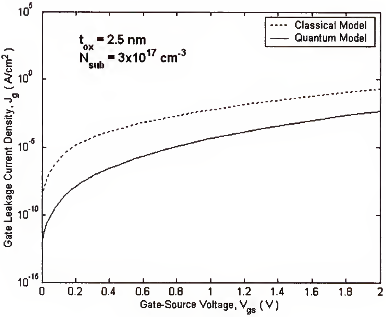


(b)

Figure 7.3 Quantum effects on (a) the inversion charge density Q_{n0} versus the gate-source voltage V_{gs} and (b) the inversion layer capacitance C_n versus V_{gs} for $N_{sub} = 3\times10^{17}$ cm^{-3} and 3×10^{18} cm^{-3}. (t_{ox} = 2.5 nm, V_{FB} = -0.9 V, $E_{ij} = E_{10}$, $N_{it} = 2\times10^{11}$ cm^{-2}, $N_{poly} = 2\times10^{20}$ cm^{-3}, T = 300 K)

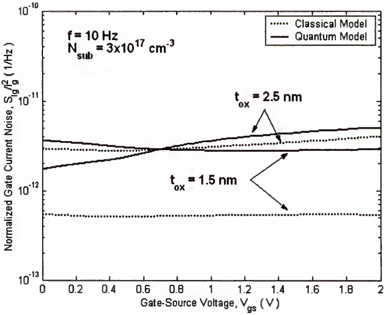


(a)

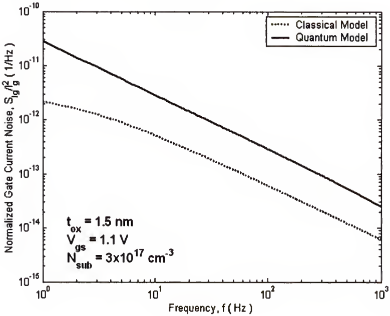


(b)

Figure 7.4 Quantum effects on (a) the oxide voltage V_{ox} versus the gate-source voltage V_{gs} and (b) the gate leakage current density J_g versus V_{gs}. (t_{ox} = 2.5 nm, N_{sub} = 3×10^{17} cm^{-3}, V_{FB} = -0.9 V, E_{ij} = E_{10}, N_{it} = 2×10^{11} cm^{-2}, N_{poly} = 2×10^{20} cm^{-3}, T = 300 K)

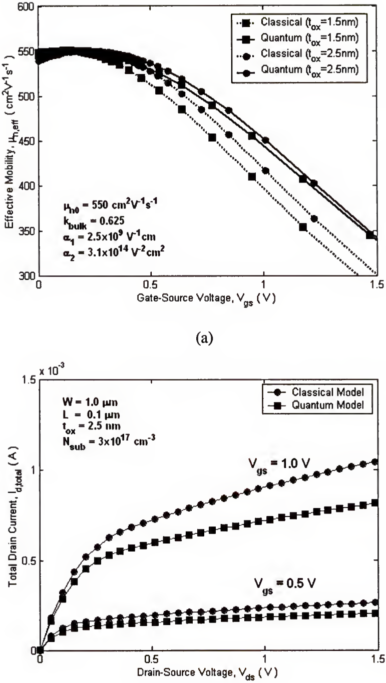


(a)



(b)

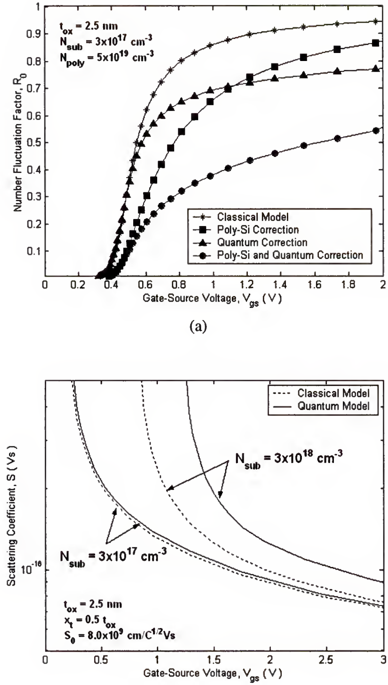
Figure 7.5 Quantum effects on (a) the normalized 1/*f* noise of gate leakage current S_{Ig}/I_g versus the gate-source voltage V_{gs} for two oxide thickness values and (b) the normalized 1/*f* noise of gate leakage current S_{Ig}/I_g versus the frequency *f*. ($N_{sub} = 3\times10^{17}$ cm^{-3}, V_{FB} = -0.9 V, $E_{ij} = E_{10}$, $N_{it} = 2\times10^{11}$ cm^{-2}, $N_{poly} = 2\times10^{20}$ cm^{-3}, T= 300 K)



(a)

(b)

Figure 7.6 Quantum effects on (a) the electron effective mobility $\mu_{n,eff}$ versus the gate-source voltage V_{gs} for two oxide thickness values and (b) the total drain current $I_{d,total}$ versus the drain-source voltage V_{ds} for two gate-source voltages ($N_{sub} = 3\times10^{17}$ cm^{-3}, $V_{FB} = -0.9$ V, $E_{ij} = E_{10}$, $v_{sat} = 8\times10^6$ cm/s, $R_{s,d} = 10\ \Omega$, $k_{bulk} = 0.625$, $T = 300$ K)



(a)

(b)

Figure 7.7 Quantum effects on (a) the number fluctuation factor R_0 versus the gate-source voltage V_{gs} with the poly-silicon depletion effects and (b) the scattering coefficient S versus the gate-source voltage V_{gs} for two substrate doping densities ($t_{ox} = 2.5$ nm, $V_{FB} = -0.9$ V, $E_{ij} = E_{10}$, $T = 300$ K)

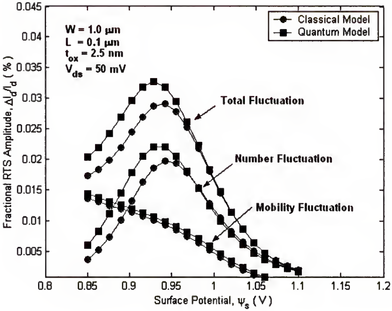
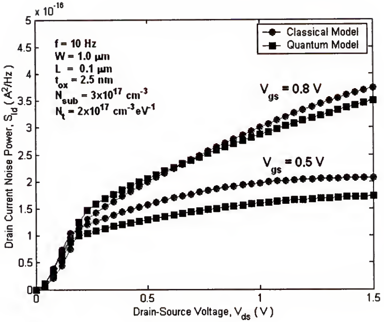


Figure 7.8 Quantum effects on the fractional RTS amplitude $\Delta I_d/I_d$ versus the surface potential ψ_s (t_{ox} = 2.5 nm, N_{sub} = 3×10^{17} cm^{-3}, V_{FB} = -0.9 V, E_{ij} = E_{10} , S_0 =8×10^{9} $cm/C^{1/2}Vs$, k_{bulk} = 0.625, T = 300 K)



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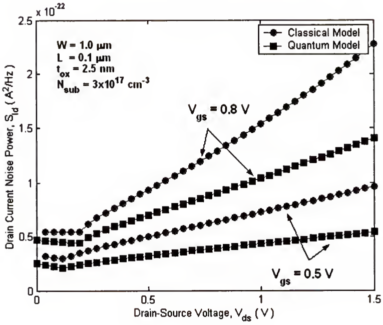


(b)

Figure 7.9 Quantum effects on (a) the 1/*f* noise power of drain current versus the drain-source voltage V_{ds} and (b) the thermal noise power of drain current versus the drain-source voltage V_{ds} for two gate-source voltages ($N_{sub} = 3\times10^{17}$ cm^{-3}, $V_{FB} = -0.9$ V, $E_{ij} = E_{10}$, $v_{sat} = 8\times10^{6}$ cm/s, $R_{s,d} = 10\ \Omega$, $k_{bulk} = 0.625$, $T = 300$ K)

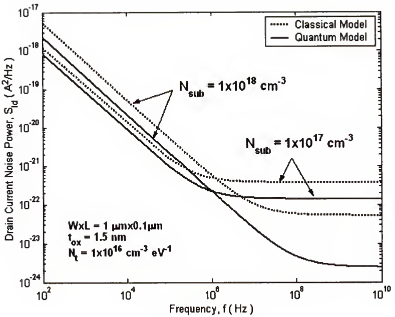


Figure 7.10 Quantum effects on the total noise power of drain current versus the frequency f for two substrate doping concentrations (V_{FB} = -0.9 V, E_{ij} = E_{10}, $v_{sat} = 8\times10^6$ cm/s, $R_{s,d}$ = 10 Ω, k_{bulk} = 0.625, T = 300 K)

between the classical and QM model increases with decreasing oxide thickness. Figure 7.5 (b) clearly shows a $1/f^{\gamma}$ frequency dependence with the power factor γ close to unity.

On the basis of the inversion charge model including QM effects, the drain current and noise model is evaluated for ultrathin oxide MOS device ($t_{ox} = 1.5\sim2.5$ nm). As shown in Figure 7.6 (a), the QM effects on the effective mobility become noticeable with thinner oxide thickness and higher gate-source voltage. Figure 7.6 (b) illustrates that QM models give lower drain current values with respect to the classical model and QM effects become more significant in the saturation region. Prior to the evaluation of $1/f$ noise model, it is necessary to investigate QM effects on the RTS fluctuations which are the origin of $1/f$ noise. The QM and polysilicon depletion effects on the number fluctuation factor R_0 versus the gate-source voltage are plotted in Figure 7.7 (a). The QM and polysilicon depletion effects are appreciably enhanced in the strong inversion. Figure 7.7 (b) shows QM effects on the scattering coefficient S as a function of the gate-source voltage. For higher substrate doping concentration, QM effects become more noticeable. Based on number and mobility fluctuations, the RTS amplitude versus the surface potential is evaluated using the QM correction charge model, as shown in Figure 7.8. Note that in the case of number fluctuations, the classical and QM models exactly coincide in the strong inversion and somewhat deviate in the weak inversion. For the evaluation of $1/f$ drain current noise, it is assumed that the number fluctuation appreciably contributes to the total current noise. As illustrated in Figure 7.9 (a), the classical and QM models of $1/f$ drain current noise behave in a qualitatively similar fashion to the RTS noise in the weak and strong inversion, showing the deviation in the saturation region. Figure 7.9 (b) illustrates the thermal noise spectral power density of drain current as a function of the drain-source voltage for different gate-source voltage. It is seen that QM effects are also important to the thermal noise modeling. As shown in Figure 7.10, it is confirmed that for higher doping concentration and thinner oxides, QM effects in the inversion layer should be considered for accurate noise modeling of nanoscale MOSFETs.

7.6 Conclusion

The current and noise models accounting for QM effects in nanoscale MOSFETs were presented. Based on the BSIM framework, simple and analytical models were formulated by considering the QM effects due to the lowest energy level in the inversion layer. The inversion charge parameters were studied and treated quantum-mechanically, because good modeling of current and noise depends strongly on the accurate estimate of the inversion charge due to QM effects. The gate leakage current and noise models were evaluated by using the quantum correction model for the oxide voltage and oxide thickness. By accounting for the QM effects through the inversion charge density model, the quantum models of the drain current and noise were obtained and compared with the classical models. The simulation results showed that 1) the quantum correction of the oxide thickness is essential to the accurate prediction of the gate leakage current and noise model, 2) QM effects on the *1/f* noise and the thermal noise of drain current is significant in the saturation region, similar to the drain current characteristics, and 3) QM effects on the noise model become more pronounced for higher doing concentration and thinner oxide thickness. Therefore, as the MOS devices are scaled down to nanometer regime, existing current and noise models should incorporate more accurate, physics-based descriptions which account for quantization effects observable in the inversion layer.

CHAPTER 8
COMPACT NOISE MODELING AND IMPLEMENTATION

8.1 Introduction

Aggressive downscaling of MOSFETs has been driven by significant advances in CMOS technologies, leading to increasing demands for compact model (CM) development. The compact modeling of MOS devices is critical for the computer-aided design (CAD) of digital and analog VLSI circuits [Joa98, Tsi94]. There are several recently published compact models of MOSFETs, such as the BSIM4 model from Berkeley [Ber01], the MM11 model from Philips [Phi01], the EKV model [Enz96], and the MISNAN model [Boo91]. Among them, BSIM3v3 was selected as the first and public domain MOSFET model for standardization by the compact model council (CMC). Although BSIM4 has demonstrated the capability to predict sub-micron device characteristics, it is still necessary to develop a generic and practical model flexible to the significant changes in modern CMOS devices with nanometer dimensions [Ber01]. Especially, an accurate and physical noise modeling is essential for the use of modern CMOS devices, because the noise becomes increasingly larger with shrinking devices [Cel99, Sim99]. With the downscaling of gate oxide thickness, the effects of the gate tunneling current noise become significantly critical, and should thus be incorporated to accurately predict the overall noise performance [Mom98]. The noise models should describe all kinds of the noise sources, including the important physical effects of nanoscale MOSFET, such as quantum mechanical effects in the inversion layer [And82].

Table 8.1 Comparison of BSIM4 and UF_Noise for noise models

MOS Noise Model		BSIM4	UF_Noise
Gate leakage current noise	1/*f* noise model	Not included	Implemented
	Shot noise model	Not included	Implemented
1/*f* noise of drain current	Number of trap-related parameters	3	2
	Trapping-detrapping process	Tunneling	Tunneling-thermal
	Trap distribution	Uniform	Over space and energy
	Frequency exponent	Default (1.0)	Bias-dependent
	Parasitic resistance	Not included	Included
Correlation noise		Not included	Developed
QM correction noise		Not included	Developed
Applicable oxide thickness		> 3.0 nm	< 3.0 nm

As shown in Table 8.1, the BSIM does not contain the noise model of gate leakage tunneling current as well as the correlation noise model between the gate and drain, which are no longer negligible in untrathin oxide MOSFETs. In addition, BSIM noise model of drain current has several drawbacks which are physical limitations for trapping-detrapping process, unrealistic trap distribution over the energy and space, no capability of explaining the gate bias dependence of the frequency exponent, and no consideration of parasitic series resistance [Hun90a, Hun90b]. In order to overcome the problems mentioned above, we have developed the physics-based compact model of the gate leakage current and noise in ultrathin gate oxide MOSFETs, in Chapter 2 and 3. It was found for nitrided oxide that the results simulated by the proposed current model have better agreement with the experimental results than those under BSIM model. Also, the newly proposed noise model can accurately predict the excess noise behavior of MOS transistors with ultrathin gate oxide. In addition, for the overall noise performance of ultrathin oxide MOSFETs at low frequencies, the correlation noise between the gate and the drain should be modeled, and the noise model has been developed in Chapter 5. Furthermore, we have proposed the newly developed drain current noise model and QM correction model, based on sound physical reasoning, as shown in Chapter 6 and 7.

In this Chapter, the physics-based compact noise model will be expressed in such a way that the models incorporate important physical effects and are suitable for circuit simulators, including QM effects on the gate leakage current noise, the drain current noise, and the correlation noise. An emphasis on the trap-related parameters of noise models is laid to make the models adaptable to the variations in different process technologies and to make its parameters easily extractable from measured data. With the help of an accurate and generally applicable compact noise model, we can successfully implement the compact noise models into BSIM format.

8.2 UF_Noise : Gate Leakage Current and Noise Models

8.2.1 Model Implementation in BSIM4

The gate leakage current model is based on the inelastic trap-assisted tunneling process (ITAT). The model describes electrons tunneling to deep-lying trap states and, immediately, released to positions deeper than the original position, and subsequently tunneling to the gate [Lee02]. In terms of trap-related parameters, X_t , ϕ_t, *CCS*, and *NOID*, defined in Table 8.2, the expressions for the gate leakage current density with the drain-to-source voltage $V_{ds}= 0$ are rewritten as

$$J_{g0} = \frac{q^2}{16\pi^2\hbar\varepsilon_{ox}} \cdot CCS \cdot NOID \cdot \frac{\dfrac{C(\phi_b, X_t, F_{ox1})}{\phi_b} \cdot \exp\left[-\dfrac{4\sqrt{2m_{ox}}}{3q\hbar} \dfrac{\phi_b^{3/2}}{F_{ox1}} \beta(\phi_b, X_t, F_{ox1}) \right]}{1 + \dfrac{\phi_t}{\phi_b} \cdot \dfrac{C(\phi_b, X_t, F_{ox1})}{C(\phi_t, t_{ox} - X_t, F_{ox2})} \cdot \exp\left\{ -\dfrac{4\sqrt{2m_{ox}}}{3q\hbar} \left[\dfrac{\phi_b^{3/2}}{F_{ox1}} \beta(\phi_b, X_t, F_{ox1}) - \dfrac{\phi_t^{3/2}}{F_{ox2}} \beta(\phi_t, t_{ox} - X_t, F_{ox2}) \right] \right\}} \tag{8.1}$$

with

$$\phi_t = \phi_b - qF_{ox1}X_t + E_{loss} \tag{8.2a}$$

$$F_{ox1} = F_{ox} + \frac{t_{ox} - X_t}{t_{ox}} \cdot \frac{q^2 NOID}{\varepsilon_{ox}}, \qquad F_{ox2} = F_{ox} - \frac{X_t}{t_{ox}} \cdot \frac{q^2 NOID}{\varepsilon_{ox}} \tag{8.2b}$$

$$\beta(\phi_b, X_t, F_{ox1}) = 1 - \left(1 - q\frac{X_t}{\phi_b} F_{ox1}\right)^{3/2}, \quad \beta(\phi_t, t_{ox} - X_t, F_{ox2}) = 1 - \left(1 - q\frac{t_{ox} - X_t}{\phi_b} F_{ox2}\right)^{3/2} \tag{8.2b}$$

where q is the electron charge, $\hbar$ is the reduced Planck constant, ε_{ox} is the oxide dielectric constant, ϕ_b is the Si-SiO$_2$ barrier height, m_{ox} is the effective mass of tunneling carriers, t_{ox} is the oxide thickness, E_{loss} is the energy loss, $F_{ox1,2}$ is the local electric field, and C is the correction function. The equations includes the effects of charge stored in the trap states and the dependence of the energy loss on the oxide electric field [Lee02].

Table 8.2 Trap-related parameters of noise model of gate leakage current

Symbols	Description	Default	Unit
X_t	Trap distance from Si-SiO$_2$ interface	0.5 t_{ox}	nm
ϕ_t	Barrier height of the oxide trap states	2.5	eV
CCS	Capture cross section	5.0×10^{-14}	cm^2
NOID	Oxide slow trap density	2.0×10^{12}	cm^{-2} eV^{-1}
NOIE	Oxide fast trap density	2.0×10^{12}	cm^{-2} eV^{-1}

The dependence of gate leakage current on the drain-source voltage is described by the source-drain partition model which has been already implemented in BSIM4 [Cao00]. The gate tunneling current is given by

$$I_g(V_{gs},V_{ds}) = \frac{J_{g0}WL\left(1-\exp(-B^*KL)\right)}{B^*KL} \tag{8.3}$$

with

$$B^* = \frac{P_{igcd}t_{ox}}{V_{gs}^2}\cdot\frac{8\pi\sqrt{2qm_{ox}}\phi_b^{3/2}}{3h}, \quad K = \frac{\left(V_{gs}-V_T-0.5V_{ds}\right)\cdot V_{ds}}{\left(V_{gs}-V_T\right)L} \tag{8.4}$$

where h is the Planck constant, W is the channel width, L is the channel length, P_{igcd} is a fitting parameter with a default value of 1, V_T is the threshold voltage, and V_{gs} is the gate-to-source voltage.

One possible mechanism for $1/f^\gamma$ noise contribution is for traps to affect locally the barrier height or shape due to thermal noise of the frequency-dependent conductance of the oxide slow traps [Ghi87, Kle78]. This fluctuation in turn modulates the tunneling transmission, and causes the fluctuation in the tunneling current. Three assumptions are made in implementing the $1/f^\gamma$ noise model of gate leakage current into BSIM4. 1) The oxide slow traps are uniformly distributed over the energy and space, 2) The parallel trap conductance and capacitance is constant over low frequencies, and 3) The carrier tunneling is effective for trap levels around the quasi-Fermi level. Thus, the $1/f^\gamma$ noise model of gate leakage current can be simplified as

$$S_{I_g}^{LF}(f)=\frac{16kTm_{ox}t_{ox}^2}{9\pi\hbar^2q^2WL}\cdot\frac{\dfrac{q^2NOID}{2\lambda_tX_t}}{\left[\dfrac{q^2NOID}{2\lambda_tX_t}\right]^2+\left[C_{ox}+q^2NOID\right]^2}\cdot\frac{I_g^2(V_{gs},V_{ds})}{f}\cdot\frac{1}{V_{ox}^4}\times$$
$$\left\{\sqrt{\phi_b(\phi_b-qV_{ox})}\left[8\phi_b(\phi_b-qV_{ox})-3q^2V_{ox}^2\right]-2\left[2\phi_b^2(2\phi_b-3qV_{ox})+q^3V_{ox}^3\right]\right\} \tag{8.5}$$

with

$$V_{ox}=V_{gs}-V_{FB}-\psi_s-V_{poly} \tag{8.6}$$

where $\lambda_t=2\sqrt{2m_{ox}\phi_b}/\hbar$, f is the frequency, C_{ox} is the oxide capacitance, V_{ox} is the oxide voltage, ψ_s is the surface potential, V_{FB} is the flat-band voltage, and V_{poly} is the polysilicon voltage drop.

The mechanism for shot noise associated with generation-recombination process can be explained by carrier transport based on trap-assisted tunneling [Ian00, Lee02]. The generation rate, i.e., the transition rate from the substrate and the gate to the unoccupied trap in the oxide, and recombination rate, i.e., the transition rate from the occupied trap to the substrate and the gate, are caused by the statistical occupancy fluctuation of fast oxide traps in the oxide. The shot noise model is given by

$$S_{I_g}^{shot}(f)=2qI_g\cdot F^{Fano} \tag{8.7}$$

with

$$F^{Fano}=1-\frac{2}{\tau_{fast2}}\cdot\frac{\tau_{fast}}{1+4\pi^2f^2\tau_{fast}^2}+\frac{2}{\tau_{fast2}^2}\cdot\frac{\tau_{fast}^2}{1+4\pi^2f^2\tau_{fast}^2} \tag{8.8a}$$

$$\frac{1}{\tau_{fast}}=\frac{1}{\tau_{fast1}}+\frac{1}{\tau_{fast2}} \tag{8.8b}$$

$$\frac{1}{\tau_{fast1}} = \pm 0.5 \cdot q \cdot CCS \cdot NOIE \cdot \frac{\partial g}{\partial N} \tag{8.8c}$$

$$\frac{1}{\tau_{fast2}} = \pm 0.5 \cdot q \cdot CCS \cdot NOIE \cdot \frac{\partial r}{\partial N} \tag{8.8d}$$

where F^{Fano} is the Fano factor, $\tau_{fast1,2}$ is the local time constants, N is the total number of carriers, and g and r are the uniform generation and recombination rate, respectively. The signs of Equations (8.8c) and (8.8d) depend on the positive or negative correlation between tunneling current components. As illustrated in Figure 8.1, for example, different signs of the time constants lead to enhanced shot noise.

Due to the quantized energy levels in the inversion layer, the peak charge density is situated at a distance away from the Si-SiO$_2$ interface. This results in the enhancement in the oxide thickness and the reduction in the oxide voltage. As shown in Chapter 7, therefore, the quantum effects are taken into account by using the correction for the oxide thickness, t_{ox}^{QM}, and the oxide voltage, V_{ox}^{QM}, as follows

$$t_{ox}^{QM} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{si}} x_n^{QM}(\psi_s) \tag{8.9a}$$

$$V_{ox}^{QM} = V_{gs} - V_{FB} - \psi_s^{QM} - V_{poly} \tag{8.9b}$$

where x_n^{QM} is the average centroid position from the interface and t_{ox}^{QM} is the QM corrected surface potential, as defined in Chapter 7.

8.2.2 Benchmark Tests

For the practical application of the compact noise model of gate leakage current, the models are implemented into BSIM4 in public domain, as shown in Figure 8.2.

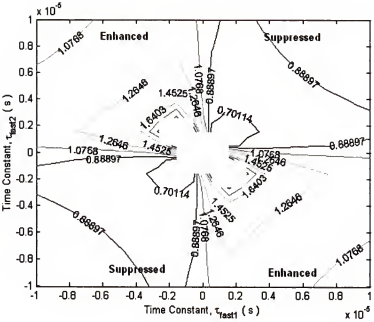


Figure 8.1 Enhancement and suppression in the Fano factor, depending on the signs of local time constants ($f = 10$ kHz)

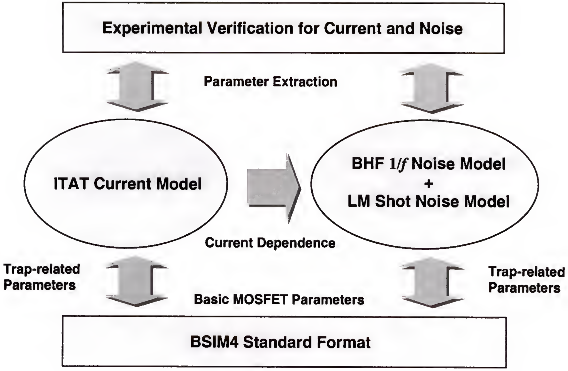
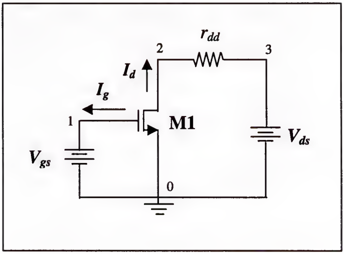
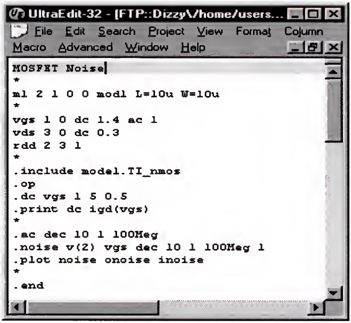


Figure 8.2 Implementation of the gate leakage current and noise models into the BSIM4 public domain platform



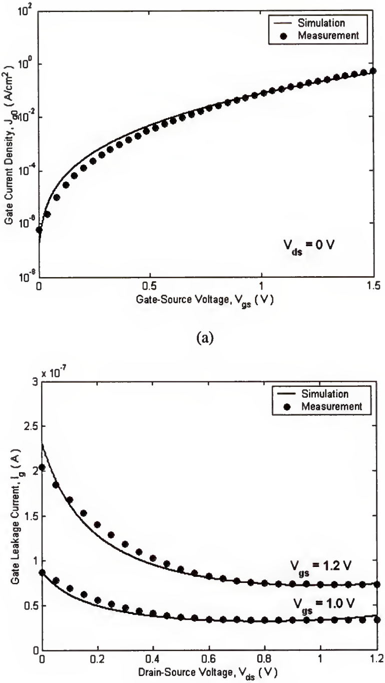
(a)


UltraEdit-32 - [FTP::Dizzy\/home/users...
File Edit Search Project View Format Column
Macro Advanced Window Help

```
MOSFET Noise
*
m1 2 1 0 0 mod1 L=10u W=10u
*
vgs 1 0 dc 1.4 ac 1
vds 3 0 dc 0.3
rdd 2 3 1
*
.include model.TI_nmos
.op
.dc vgs 1 5 0.5
.print dc igd(vgs)
*
.ac dec 10 1 100Meg
.noise v(2) vgs dec 10 1 100Meg 1
.plot noise onoise inoise
*
.end
```

(b)

Figure 8.3 Benchmark test of the noise model of gate leakage current. (a) a test circuit of a single MOSFET and (b) an input deck to simulate the gate leakage current noise



(a)

(b)

Figure 8.4 Comparison of the benchmark test results and measured data of the gate leakage current. (a) the current density versus the gate-source voltage, and (b) the simulated current versus the drain-source voltage for different gate-source voltages ($W = 10\ \mu\text{m}$, $L = 10\mu\text{m}$, $t_{ox,eq} = 2.2$ nm, $NOID = 2\times10^{12}\ \text{cm}^{-2}\text{eV}^{-1}$).

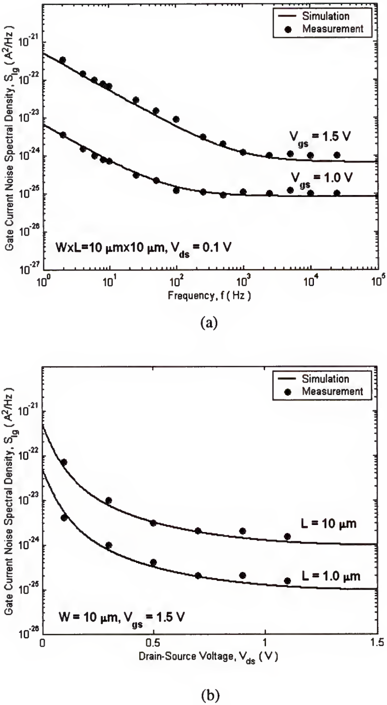


Figure 8.5 Comparison of the benchmark test results and measured data of the gate leakage current noise. (a) the noise characteristics as a function of frequency for different gate-source voltages and (b) the simulated noise characteristics as a function of drain-source voltage for two channel lengths ($t_{ox,eq} = 2.2$ nm, *NOID=NOIE* = 2×10^{12} $cm^{-2}eV^{-1}$)

The basic device parameters are also used for the current and noise models, but the trap-related parameters are newly introduced into simulators. The validation for the compact model is derived from the comparisons of simulation results and measurements. All tests are to be done using a test circuit of a single MOSFET, as depicted in Figure 8.3 (a). An input deck in SPICE format is provided in Figure 8.3 (b). Figure 8.4 (a) and (b) show the comparison of the test results and measured data of gate leakage current as a function of gate-source voltage and drain-source voltage, respectively. It is observed that the simulation results have good agreement with measurements. Also, Figure 8.5 (a) and (b) illustrate the noise characteristics as a function of frequency for different gate-source voltages and as a function of drain-source voltage for two channel lengths, respectively. It is also verified that the compact noise model can accurately predict the noise behavior over the frequency and bias ranges. As shown in Figure 8.5 (b), the downscaling of the channel length reduces the gate leakage current noise at a given oxide thickness. However, since the drain current noise increases with downscaling of channel length, a trade-off is needed to optimize the overall noise performance.

8.3 UF_Noise : Drain Current and Correlation Noise Models

8.3.1 Drain Current Noise Model

In order to explain the $1/f^{\gamma}$ noise of drain current in ultrathin oxide MOSFETs, the tunneling assisted-thermally activated (TATA) time constant model is employed, which is physically consistent with the gate leakage tunneling process [Lee02, Tew94]. Since the noise is strongly affected by trap-related properties, the noise model accounts for a realistic description of trap distribution. In addition, the model should include the effects of the two-dimensional electric fields, the parasitic resistance, the doping profile, and the mobility degradation on the noise behavior, as described in Chapter 6. The QM correction noise model can be obtained by accounting for the QM effects through the in the oxide capacitance, the threshold voltage, and the drain current in the charge density parameters as well as the gate oxide thickness [Ma01]. The QM correction model for $1/f^{\gamma}$ drain current noise in the linear region, accounting for all effects mentioned above, is given by

$$S_{I_d,lin}^{LF}(f) = \frac{qkT \cdot I_d^{QM} \cdot t_{ox}^{QM}}{WL^2 \varepsilon_{ox}\left(1 - \frac{V_{gs} - V_{T0}}{4\phi_b / q}\right)\lambda_{tun,eff}(0.5 + k_{bulk}) \cdot [2\pi\tau_{eff0} \exp(\lambda_{th,eff} E_{fn})]^{(\gamma-1)} \cdot f^{\gamma} \cdot \cos\left[\frac{\pi}{2}(\gamma - 1)\right]} \quad (8.10)$$
$$\times [N_{TA} A^*(Q_{n1,2}^{QM}, Q_{a,b}^{QM}) + N_{TB} B^*(Q_{n1,2}^{QM}, Q_{a,b}^{QM}) + N_{TC} C^*(Q_{n1,2}^{QM}, Q_{a,b}^{QM})]$$

with

$$Q_{n1}^{QM} = C_{ox}^{QM}\left(V_{gs} - R \cdot I_d^{QM} - V_{T0}^{QM}\right) \quad (8.11a)$$

$$Q_{n2}^{QM} = C_{ox}^{QM}\left(V_{gs} - R \cdot I_d^{QM} - V_{T0}^{QM} - (0.5 + k_{bulk})(V_{ds} - 2R \cdot I_d^{QM})\right) \quad (8.11b)$$

$$Q_a^{QM} = -2\left[\frac{\varepsilon_{si}}{\beta_1} + C_{ox}^{QM}\left(V_{gs} - R \cdot I_d^{QM} - V_{FB} - \psi_s\right)\right], \qquad Q_b^{QM} = -\frac{\beta_2 I_d^{QM}}{\mu_{n0} W} \quad (8.11c)$$

where V_{T0} is the threshold voltage with $V_{ds} = 0$ V, k_{bulk} is the bulk charge parameter, R is the parasitic resistance, β_1 and β_2 are the mobility parameters, μ_{n0} is the maximum mobility in the inversion layer, τ_{eff0} is an effective attempt time constant, N_{TA}, N_{TB}, and N_{TC} depend on the trap distribution in the oxide, and $\lambda_{th,eff}$ and $\lambda_{tun,eff}$ are an exponential factor of thermal activation process and tunneling process, respectively. Unlike BSIM noise model, A^*, B^*, and C^* are not empirical constants but are analytical expressions as a function of V_{gs} and V_{ds}, as described in Chapter 6.

In the saturation region, the noise power spectral density is expressed as the sum of the noise components due to the triode region, *L*-L_{sat}, and the pinch-off region, L_{sat}, and is given by

$$S^{LF}_{I_d,sat}(f) = S^{LF}_{I_d,lin}(f)\Big|_{V_d=V_{dsat}} + S^{LF}_{I_d,Lsat}(f) \tag{8.12}$$

with

$$S^{LF}_{I_d,Lsat}(f) = \frac{qkT\cdot\left(I_d^{QM}\right)^2}{WL^2\left(1-\dfrac{V_{gs}-V_{T0}}{4\phi_b/q}\right)\lambda_{tun,eff}\left[2\pi\tau_{eff0}\exp\left(\lambda_{th,eff}E_{fn}\right)\right]^{(\gamma-1)} f^{\gamma}\cos\left[\dfrac{\pi}{2}(\gamma-1)\right]} \tag{8.13a}$$
$$\times\left[N_{TA}A^*_{Lsat}(Q^{QM}_{n,sat}) + N_{TB}B^*_{Lsat}(Q^{QM}_{n,sat}) + N_{TC}C^*_{Lsat}(Q^{QM}_{n,sat})\right]\cdot L_{sat}$$

$$Q^{QM}_{n,sat} = C^{QM}_{ox}\left(V_{gs} - RI_d^{QM} - V_{T0}^{QM} - (0.5+k_{bulk})(V^{QM}_{dsat} - 2RI_d^{QM})\right) \tag{8.13b}$$

where V_{dsat} is the drain saturation voltage, and A^*_{Lsat}, B^*_{Lsat}, and C^*_{Lsat} are analytically expressed as a function of V_{gs} and V_{dsat}.

8.3.2 Comprehensive noise model

Due to the presence of the gate leakage current in ultrathin oxide MOSFETs, the comprehensive noise performance at low frequencies is evaluated by taking into account the cross correlation coefficient, $C^{LF}(f)$, between the drain and the gate current noise, and is expressed as a function of the current ratio, $\lambda_p = I_g / I_d$, and the noise ratio, $S^{LF}_{I_g}(f) / S^{LF}_{I_d}(f)$, as follows

$$C^{LF}(f)=\frac{\frac{\lambda_p}{(1+\lambda_p)(1-\lambda_p)}\left[1-\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]+\frac{1}{1+\lambda_p}\left[\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]}{\sqrt{\left\{\frac{\lambda_p^2}{(1+\lambda_p)^2(1-\lambda_p)^2}\left[1-\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]^2+\frac{1}{(1+\lambda_p)^2}\left[\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]^2+\frac{(1+\lambda_p^2)}{(1+\lambda_p)^2(1-\lambda_p)}\left[\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]\left[1-\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]\right\}}} \tag{8.14}$$

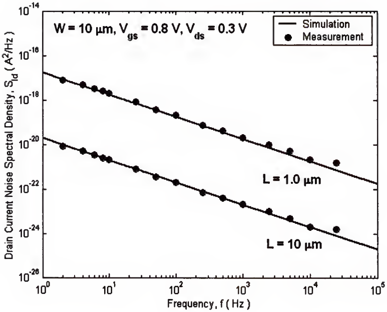
In addition to the influence of the correlation on the low frequency noise performance, the shot noise due to the gate leakage current, $S_{I_g}^{shot}(f)=2qI_gF^{Fano}$, has an impact on the noise behavior, and thus should be incorporated into the minimum noise figure $F_{\min}^{LF}(f)$ as follows [Cap88, Puc74]

$$F_{\min}^{LF}(f)=1+\frac{S_{I_d}^{LF}(f)}{2kTg_{mg}^2}\sqrt{(2\pi fC_{gs})^2\left[1-(C^{LF})^2\right]\cdot\left[\frac{g_{mg}}{g_g}\frac{S_{I_g}^{LF}(f)}{S_{I_d}^{LF}(f)}\right]+\frac{2qF^{Fano}I_gg_{mg}^2}{S_{I_d}^{LF}(f)}} \tag{8.15}$$

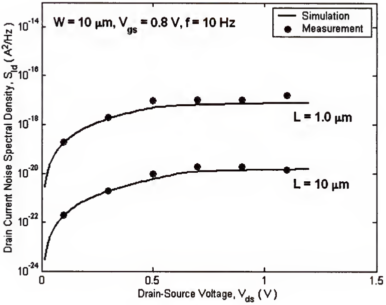
where $g_{mg}=\partial I_d/\partial V_{gs}$ is the transconductance, $g_g=\partial I_g/\partial V_{gs}$ is the gate conductance, and C_{gs} is the gate-to-source capacitance.

8.3.3 Simulation results

From the viewpoint of compact noise modeling, the model should provide an accurate prediction of noise behavior, describing all the important physical effects without an increase of parameters. For nMOSFETs with ultrathin oxide (= 2.2nm), the $1/f^{\gamma}$ noise of drain current can be accurately predicted by the expressions of (8.10) – (8.13). Figure 8.6 shows the comparison of measured data and simulation results carried out with single trap-related parameter under the assumption of uniform trap distribution in the oxide. Excellent agreements between measurement and simulation are observed

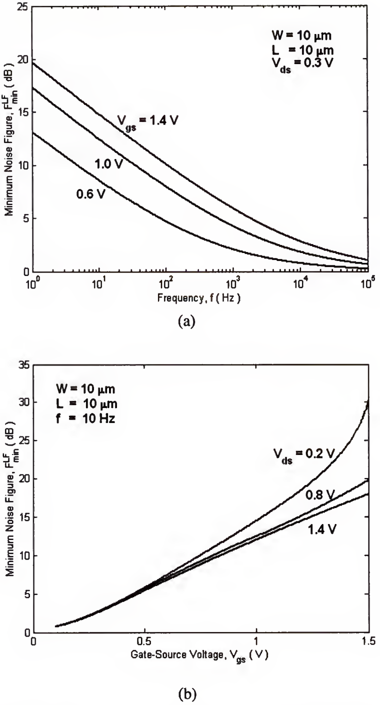


(a)



(b)

Figure 8.6 Comparison of the simulation results and measured data of the drain current noise. (a) the noise characteristics as a function of frequency for two channel lengths, (b) the noise characteristics as a function of drain-source voltage for two channel lengths, assuming that the trap is uniformly distributed. ($t_{ox,eq} = 2.2$ nm, $N_{TA} = 1\times10^{18}$ cm^{-3}eV^{-1}).



(a)

(b)

Figure 8.7 Simulation of the minimum noise figure. (a) the characteristics of minimum noise figure as a function of frequency for different gate-source voltagse, (b) the characteristics of minimum noise figure as a function of gate-source voltage for different drain-source voltages ($t_{ox,eq}$ =2.2 nm, N_{TA}= 1×10^{18} $cm^{-3}eV^{-1}$, $NOID$ = 2×10^{12} $cm^{-2}eV^{-1}$).

over the frequency and in both the linear and saturation regions for two channel lengths, as shown in Figure 8.6 (a) and (b), respectively.

For the overall noise evaluation of advanced CMOS devices, the compact noise models at low frequencies should include the correlation effects between the gate and the drain, together with the gate and drain current noise models. Unlike the capacitive coupling at high frequencies, the low frequency correlation is mainly attributed to the trap-assisted tunneling process, which is a common origin of the gate and drain current noise. With the help of an analytical expression of correlation coefficient, it is possible to evaluate the minimum noise figure, as illustrated in Figure 8.7. Figure 8.7 (a) and (b) show the characteristics of minimum noise figure as a function of frequency for different gate-source voltages V_{gs} and the gate-source voltage for different drain-source voltages V_{ds}, respectively. The increasing minimum noise figure with increasing V_{gs} and decreasing V_d can be interpreted as being due to the gate leakage current and its noise components, greatly affecting the overall noise performance at low frequencies.

8.4 Conclusion

The comprehensive and physics-based compact noise models for advanced CMOS devices were presented. The models incorporate important physical effects in nanoscale MOSFETs, such as the gate leakage current and noise, the low frequency correlation effect between the drain and the gate, the trap-related phenomena, and QM effects in the inversion layer. Especially, the gate leakage current and noise models were implemented in BSIM4 simulator and were verified with the comparison of simulation results and measurements. For ultrathin oxide MOSFETs, the drain current noise model was improved by including the tunneling assisted-thermally activated process, the realistic trap distribution, the parasitic resistance, and mobility degradation. The expression of correlation coefficient was analytically described, enabling the overall noise performance to be evaluated. With the consideration of QM effects, the comprehensive low frequency noise performance was simulated over the entire bias range. Based on the simulation results and measurements, it is found that as modern CMOS technology scales down to nanometer dimension, the noise model should be replaced by more accurate and generally applicable physics-based model.

CHAPTER 9
SUMMARY AND RECOMMENDATIONS FOR RELATED WORK

9.1 Summary

The research presented in this dissertation explored the development of physics-based compact noise models of nanoscale MOSFETs, which are applicable to circuit simulation and can be used to upgrade the existing noise models in the BSIM simulator. The models include the noise behavior due to the gate leakage current, the drain current, the cross correlation between the gate and the drain, and the quantization in the inversion layer of ultrathin oxide MOS devices. It was also demonstrated in Chapter 4 that $1/f^{\gamma}$ noise of the gate leakage current is directly applicable to extract the trap properties of an ultrathin oxide MOS structure. Especially, the compact noise model of the gate leakage current was newly implemented into BSIM4, and the utility of the modeling was verified by a comparison of the simulation results with measurements, as shown in Chapter 8.

A short description of the noise models developed in this work will be outlined and improvements are highlighted in terms of noise modeling. The models offer the following unique features :

1) For the characterization of the enhanced conduction observed in the thin nitrided oxide devices, the gate leakage current model is based on inelastic trap-assisted tunneling mechanism combined with a semi-empirical direct tunneling current model, including the effects of charge stored in the trap states and the dependence of the energy loss on the oxide field, as shown in Chapter 2.

2) A physics-based noise model of gate leakage current is developed, which is physically based on the trap-related tunneling processes, as described in Chapter 3. In order to explain the excess noise behavior, low and high frequency noise models are formulated using a barrier height fluctuation model and Lorentzian-modulated shot noise model for the gate leakage current, respectively.

3) In Chapter 5, for a comprehensive evaluation of low frequency noise performance in ultrathin gate oxide MOSFETs, the model includes the gate leakage current and the cross correlation coefficient between the drain and the gate. By using the partition noise theory and the BSIM4 partition current model, the correlation coefficient at low frequencies is modeled. The noise performance characteristics at low frequencies, such as minimum noise figure, optimum source resistance and reactance, are evaluated by introducing the frequency-dependent noise parameters, P^{LF}, R^{LF}, and C^{LF}.

4) A $1/f^{\gamma}$ drain current noise model of ultrathin oxide MOSFETs operating in both the linear and saturation regions is formulated on the basis of the tunneling assisted-thermally activated process of carriers, incorporating a realistic description of trap distributions, as shown in Chapter 6. The model incorporates the effects of the two-dimensional electric field, the parasitic resistance, the doping profile, and the quadratic mobility degradation factor on the noise behavior.

5) In Chapter 7, quantum-mechanical (QM) effects on the noise characteristics have been taken into account for the first time, extending the applicability of the model to ultrathin (≈1.5nm) MOS devices. By considering the QM effects due to the lowest energy level in the inversion layer, quantum noise models are obtained and compared

with classical models. It is observed that QM effects on the noise model become more pronounced for higher doing concentration and thinner oxide thickness.

6) With the help of analytical and physical noise models applicable to nanoscale MOSFETs, the noise models can be implemented into general-purpose circuit simulators, providing a comprehensive evaluation of noise characteristics in advanced CMOS devices.

9.2 Recommendations for Future Work

Although the noise models in this dissertation are focusing on the noise behaviors of n-channel MOSFETs, the models are equally applicable to p-channel MOSFETs if the appropriate changes for voltage polarity, barrier height, and some physical parameters are made. Nevertheless, more work has to be done on the model verification by noise measurements over the entire bias range.

As described in Chapter 3, the shot noise due to the gate leakage current is suppressed or enhanced, depending on the sign of the characteristic time constants. While the Lorentzian-modulated shot noise model can accurately predict the noise behavior, it is still necessary to identify the physical origin of transport process responsible for the shot noise. A microscopic analysis of shot noise can be done by combining Coulomb interaction with trapping-detrapping process in a MOS structure, and simulations can be performed by means of an ensemble Monte Carlo simulator self-consistently coupled with a Poisson solver [Vas02].

Besides this work on compact noise modeling, future research must explore the RTS noise modeling, the RF compact noise modeling, and low noise design. Due to the continuous downscaling of CMOS devices, it may occur that only one oxide trap with an energy within a few *kT* of the surface Fermi level exists. Under these conditions, the current fluctuations behave discretely and are known as RTS noise. The analysis of RTS noise provides the opportunity of studying the interaction of inversion carriers with interface states, and the RTS noise is also strongly correlated with the presence of an excess leakage current. Therefore, an accurate and general RTS noise model is needed to predict the noise behavior of future devices. In addition, continuous downscaling of CMOS devices makes CMOS technology a viable choice for RF applications. Nevertheless, the design of RF ICs for real products remain a challenge due to the strong constraints on noise. Particularly, for analog applications, such as front-end circuits for wireless communication, noise issues are of primary importance. This requires the development of RF compact noise models for advanced CMOS devices. Furthermore, from the practical viewpoint of optimum noise performance, the noise should be reduced as a function of the process technology [Che01b, Jay90, Lai99, Toi01], channel engineering [Che02, Chr02, Mat97, Okh99, Yos98], and circuit techniques [Blo91, Gie99, Hsu99, Klu00, Wel00].

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